

27906

2017 Nov A
Subject: MES (CBSGS)
Semester: VI
Marks: 80
Solution

- Q.1 Answer the following: [20]
- a. Drawing PSW register format – 02 marks
PSW register format explanation – 03 marks.
 - b. Definition of embedded system– 01 marks
Two applications of embedded system– 2 X 02 = 04 marks.
 - c. Explanation of 8051 stack– 02 marks
Explanation of 8051 stack instructions– 03 marks.
 - d. Flowchart for scanning and identifying the key in a 4X4 matrix keyboard by the 8051 microcontroller– 05 marks.
- Q.2
- a. Diagram showing the 8051 connection to DAC0808– 05 marks
Program to generate a square waveform at the output of the DAC– 05 marks.
 - b. Diagrams for I2C, SPI and USB bus protocols – 05 marks
Explanation for the I2C, SPI and USB bus protocols– 05 marks.
- Q.3
- a. Interrupt definition– 02 marks
Explaining the six interrupts of 8051 microcontroller– 08 marks.
 - b. Drawing the architecture of 8051 microcontroller– 04 marks
Explaining the architecture of 8051 microcontroller – 06 marks.
- Q.4
- a. Drawing TMOD register format– 01 marks
Explaining the TMOD register format– 02 marks.
Explaining various timer modes of 8051 microcontroller– 07 marks.
 - b. Writing the program to continuously transfer “ENGG” serially at 9600 baud, 8-bit data, and 1 stop bit– 10 marks to be distributed to different parts of the program.
- Q.5
- a. Explanation for the concept of RTOS– 05 marks
Explanation for interrupt latency and response time– 05 marks.
 - b. Writing “C” program to get bit P1.1 and send it to P2.2 after inverting it– 05 marks.
 - c. Diagram for demultiplexing of address and data lines of 8051 microcontroller – 03 marks.
Explanation for the diagram– 02 marks.
- Q.6 Write short notes on the following: (Any Four) [20]
- a. Scheduler and its types explanation – 05 marks

b. SCON SFR—2.5 marks. TCON SFR—2.5 marks.

c. Diagram for interfacing 7-segment LED display with 8051 microcontroller—3 marks

Explaining the diagram—2 marks

d. Power saving mode of 8051—2.5 marks

e. Power down mode of 8051—2.5 marks.

e. Embedded system design constraints explanation—5 marks.

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