Q. P. Code: 26370

[Time : 3 hours] **[Marks : 80]**

N.B.:
(1) Question number 1 is compulsory.
(2) Attempt any three questions from the remaining five questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data, wherever it is necessary.

Q.1 Solve any four questions out of five questions.
a. State and Prove De-Morgan's theorem. [05]
b. Explain reflective codes with example. [05]
c. Explain hazards in combinational circuits. [05]
d. Explain with respect to flip-flop: [05]
i. Level Triggering ii. Edge Triggering
e. Compare CMOS and TTL logic families. [05]

Q2. a. Reduce the following using K-map and implement using NAND gates. [10]
$f(A,B,C,D) = \pi M (0,2,4,5,8,9,10,12)$
Q2. b. Design Gray ($G_3G_2G_1G_0$) to Binary ($B_3B_2B_1B_0$) converter. [10]

Q3. a. Design a two bit multiplier, (A_1A_0) with (B_1B_0). [10]
Q3. b. Implement $f(A,B,C,D) = \pi M (1,2,3,5,6,7,8,12,13)$ using: [10]
i. 16:1 MUX
ii. 8:1 MUX (one only) and a NOT gate

Q4. a. Explain the operation of S-R flipflop using NAND gates. Explain race around condition. [10]
Q4. b. Explain bidirectional shift register. [05]
Q4. c. Convert JK flipflop to T flipflop. [05]

Q5. a. Design a synchronous MOD4 UP/DOWN counter using JK flipflop. [10]
Q5. b. Explain full subtractor circuit. [05]
Q5. c. Explain master-slave flipflop. [05]

Q.6. Write short notes on any four of the following: [20]
a. Steps in Quine McClusky's method
b. Counter ICs
c. Hamming Code
d. Five and Six variable K-maps
e. Design of 3 bit odd parity generator

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