Q.P. Code: 25999

Duration: 03 hours **Total marks: 80 marks**

N.B: Attempt any 4 questions out of 6 questions

Assume suitable data wherever necessary

Q.1.a) Explain how Pentium processor detects branch with branch prediction logic techniques? **[10]**

b) What is TSS? How task switching take place in 80386 processor? Give details with TSS descriptors? **[10]**

Q.2] a) Highlight on instruction level parallelism and compare with machine level parallelism? List all dependencies of ILP? **[10]**

b) Explain code cache structure, line storage algorithm and split line access with respect to Pentium processor? **[10]**

Q.3] a) Explain address translation mechanism of 80386 processor with neat diagram? **[10]**

b) Explain in order and out of order execution methods with suitable examples? **[10]**

Q.4] a) Explain Pentium cache coherency problems and give suitable solutions by appropriate write policies? **[10]**

b) With neat diagram state the features, types and advantages of Multiprocessor Organization? **[10]**

Q.5] a) Explain pipeline hazards in detail? State the types of hazards and solution mechanisms? **[10]**

b) Draw and explain timing diagram for instruction pipeline operation and show the timing diagram with the effect of a conditional branch? State the assumptions. **[10]**

Q.6] **Write short notes on any three:** **[20]**

a) Superscalar and super pipelined processors

b) SMP and CMP

c) VLIW processors

d) Privilege levels of 80386

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