

Time: 3 Hours

Marks: 80

Please check whether you have got the right question paper.

- N.B. 1) Q. No. 1 is compulsory.
 2) Attempt any three out of remaining four questions.
 3) Assume any suitable data wherever required but justify the same.
- 1 a Explain the Need & Effect of scaling. 20
 b Find resistance R_n for nMOS if electron mobility $\mu_n=560\text{cm}^2/\text{V-sec}$,
 $t_{ox}= 10 \text{ nm}$, $\epsilon_{ox}= 3.9 \times 8.85 \times 10^{-14} \text{ F/cm}$, and $V_G=3.3 \text{ Volts}$
 $V_{THn} =0.7 \text{ Volts}$ if $W=10\mu\text{m}$ $L=0.5\mu\text{m}$
 c Explain Latch-up problem in CMOS and how it can be avoided
 d Draw the circuit and explain the working for bidirectional pad
- 2 a Design CMOS inverter such that the switching threshold is $V_{th} = 1.2$ 10
 V , with the following device parameters:
 NMOS: $V_{T0,n}= 0.6 \text{ V}$ $\mu_n C_{ox}=60 \mu\text{A}/\text{V}^2$
 PMOS: $V_{T0,p}= -0.8 \text{ V}$ $\mu_p C_{ox}=20 \mu\text{A}/\text{V}^2$
 Assume $V_{DD}= 2.4 \text{ V}$ and $\lambda=0$
- b Derive expression for current in saturation region from that of the linear 10
 region current equation also explain the effect of substrate potential
 (Body Effect) on current and also discuss the effect on overall
 performance of the device.
- 3 a Explain the effect of scaling on interconnects and comment on 10
 performance of VLSI circuit.
 b Draw the schematic of carry look-ahead adder Explain how speed can 10
 be improved?
- 4 a
$$F = \frac{\quad}{a \cdot b + c \cdot d \cdot e}$$
 10
 Consider the logical function as given above
 i) Design the CMOS logic gate that provides the function.
 ii) Is it possible to find an Euler graph for the circuit? If so, construct
 the graph and also it to perform stick level layout. If not find a
 Layout strategy for the GATE.

- b For the function $Z = \overline{(A + B)(E + F)(H + I)}$ 10
(i) Domino CMOS circuit (ii) Draw an equivalent circuit for domino circuit by using equivalent transistor sizes with $W/L=30/2$ (both for NMOS and PMOS)
- 5 a Explain the Latch-up problem in CMOS with neat diagram also give the different methods to overcome the latch-up. 5
- b Compare various loads used in Inverter circuit. Draw proper diagram and compare different parameters which characterize each type of Inverters 10
- c Draw the Schematic of 6-transistor SRAM cell also the draw layout for the same 5
- 6 a Explain the clock generation and different types of clocking schemes for VLSI circuit Explain various issues of clock distribution? Explain how they are addressed? 10
- b How the cross-talk in multilayer system is modeled? 5
- c Explain Charge sharing problem and give the solution 5
