Solution for Q.P. Code: 13320
Subject: Digital Electronics (CMTRX)

Q1) a) **Shift Reg :⇒**

The binary data in register can be moved within the reg. from one FF to another. The reg. that allows such data transfer is called as shift Reg.

Data can be entered in serial or parallel form & can be retrieved in serial & parallel form.

There are four possible modes of operation.
① SISO ② SIPO ③ PISO ④ PIPO

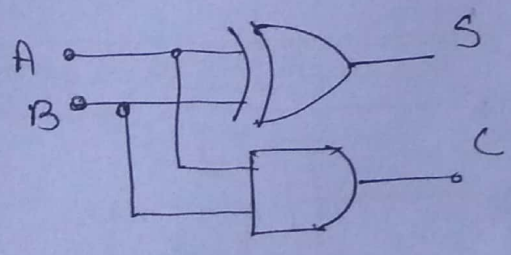
Application of shift Reg. Sequence generators.

b) Drawback of Synch. Counter.

Clock Skew.

- It is a phenomenon in synchronous digital systems in which the same sourced clock signal arrives at diff. component at different times, i.e. instanteneous diff. betn the reading of any two clocks is called their clock skew.

c) **Half Adder**



I/P		O/P	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Q1) d) **Noise Margin**

A quantitative measure of a ckt's noise immunity is called Noise Margin.

Noise Margin for CMOS : 1.45 Volts

Noise Margin for TTL : 0.4 Volts.

Q2) a) $F(A,B,C,D) = \Pi M(1,2,4,7,11,13) + d(9,15)$

$F(A,B,C,D) = \Sigma M(0,3,5,6,8,10,12,14) + d(9,15)$

AB \ CD	00	01	11	10
00	1 (0)	(1)	1 (3)	(2)
01	(4)	1 (5)	(7)	1 (6)
11	1 (12)	(13)	X (15)	1 (14)
10	1 (8)	X (9)	(11)	1 (10)

OR (using POS)

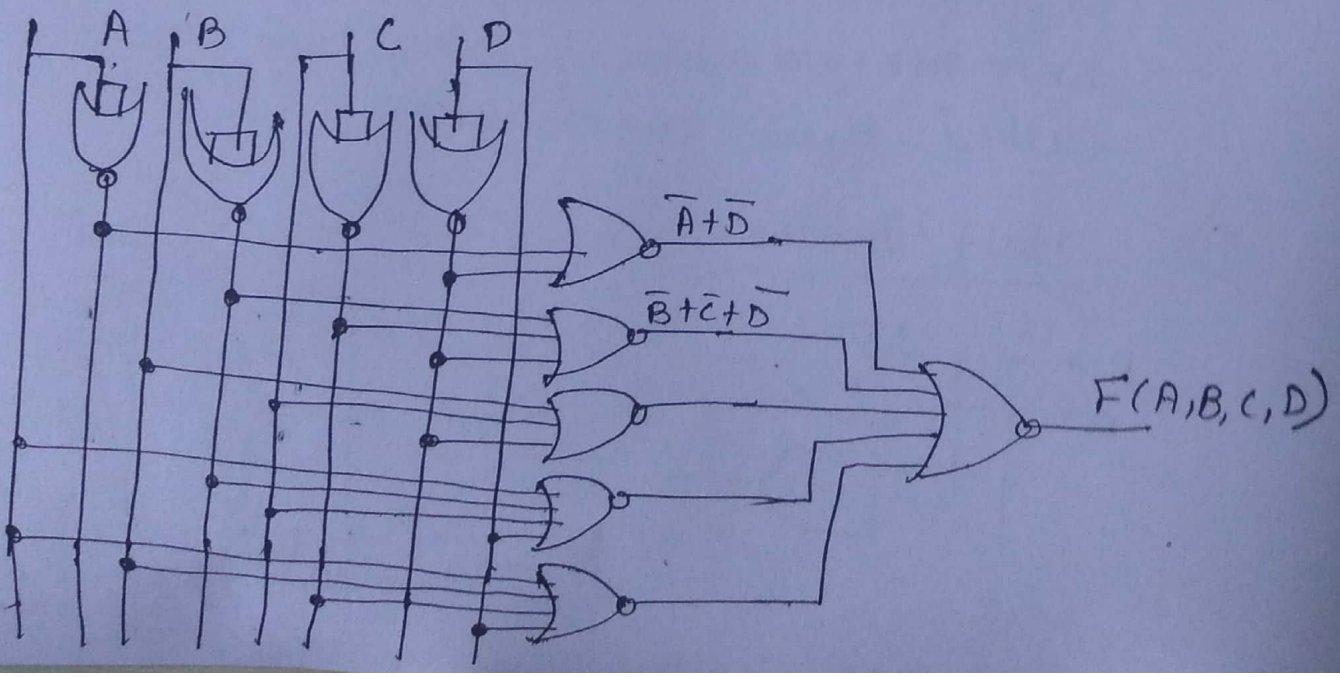
AB \ CD	00	01	11	10
00	(0)	0 (1)	(3)	0 (2)
01	0 (4)	(5)	0 (7)	(6)
11	(12)	0 (13)	0 (15)	(14)
10	(8)	0 (9)	0 (11)	(10)

$F(A,B,C,D) = (\bar{A}+\bar{D}).(\bar{C}+\bar{D}+\bar{B}).(B+C+\bar{D}).(A+\bar{B}+C+D).(A+B+\bar{C}+D)$

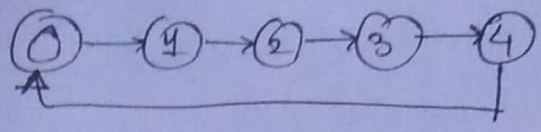
following POS :

$F(A,B,C,D) = \overline{(\bar{A}+\bar{D}).(\bar{B}+\bar{C}+\bar{D}).(B+C+\bar{D}).(A+\bar{B}+C+D).(A+B+\bar{C}+D)}$

$F(A,B,C,D) = \overline{(\bar{A}+\bar{D})} + \overline{(\bar{B}+\bar{C}+\bar{D})} + \overline{(B+C+\bar{D})} + \overline{(A+\bar{B}+C+D)}$

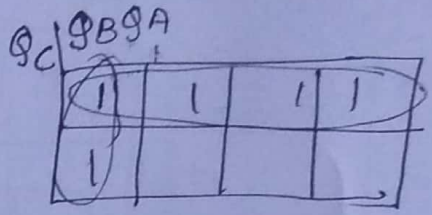


Q2) b) MOD-5 asynchronous Counter.

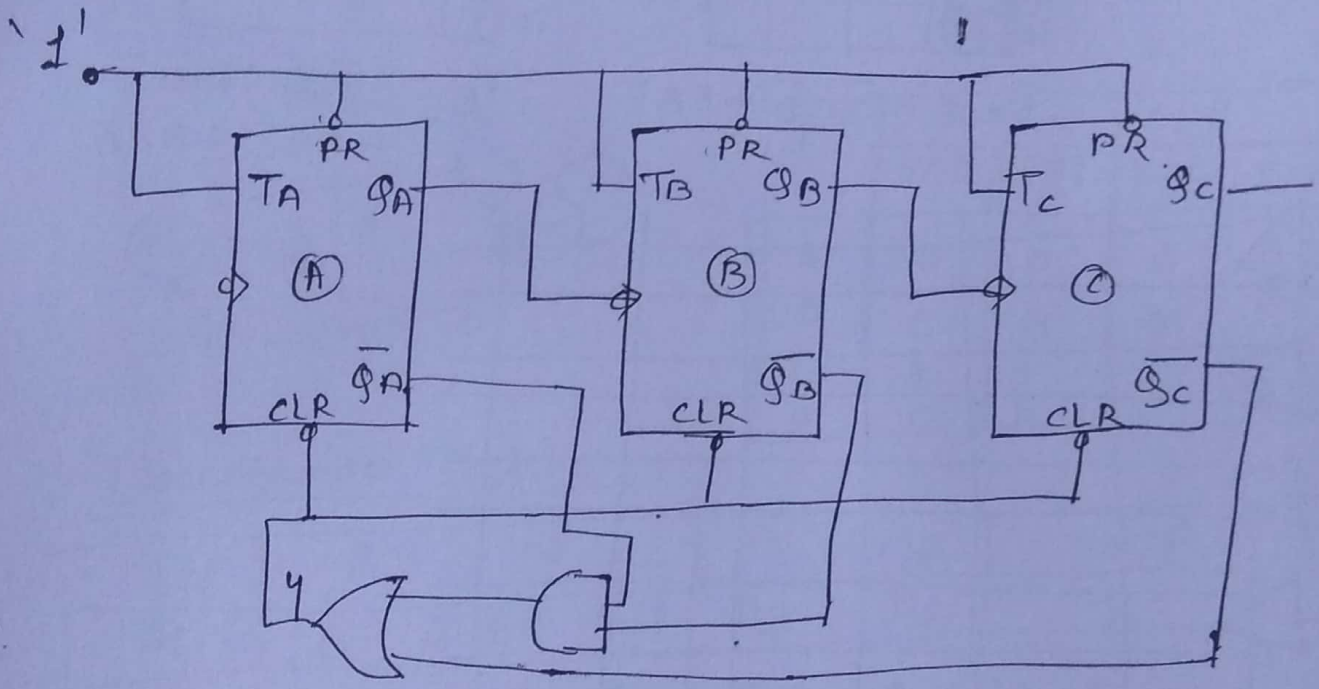


State	FF. I/P.			O/P(Y)
	Q_C	Q_B	Q_A	Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

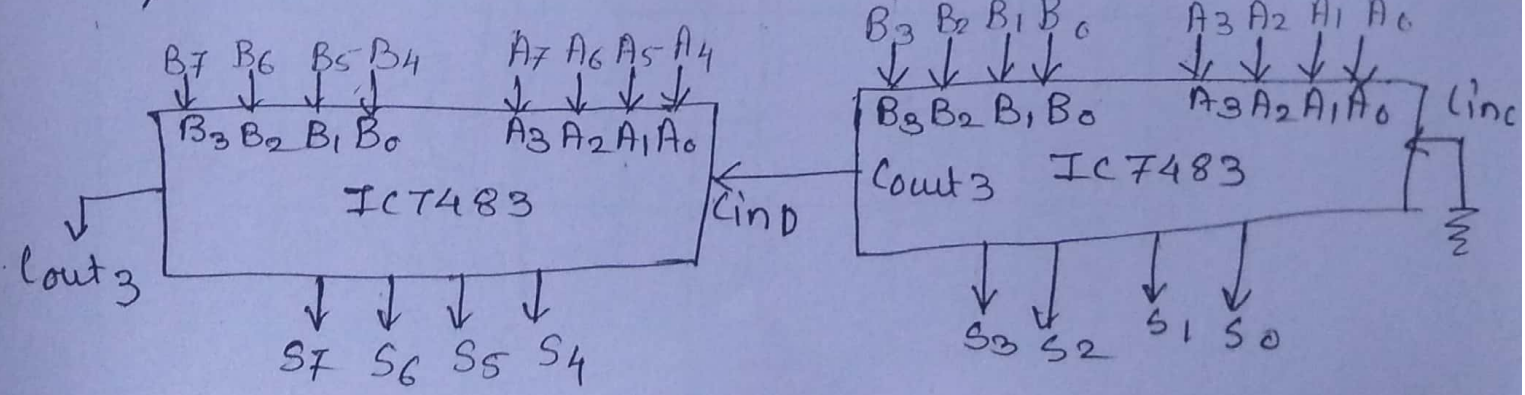
Kmap for Y.



$Y = \overline{Q_C} + \overline{Q_B}\,\overline{Q_A}$



Q3) a) 8-bit binary adder using IC 7483



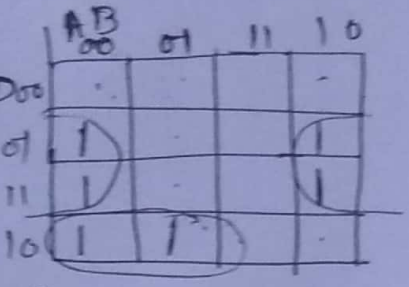
Q3 b) Here, $D = x \oplus y \oplus z$

Q4 a) $F_1 = \Sigma m(1,2,3,6,4,11)$

$F_2 = \Sigma m(2,12,13)$

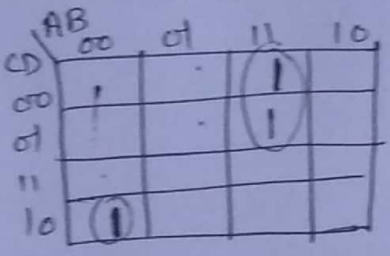
$F_3 = \Sigma m(1,2,8,12,13)$

Here, $F_1 = \bar{C}D$

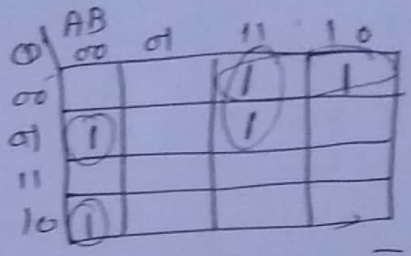


$\therefore F_1 = B\bar{D} + \bar{A}C\bar{D}$

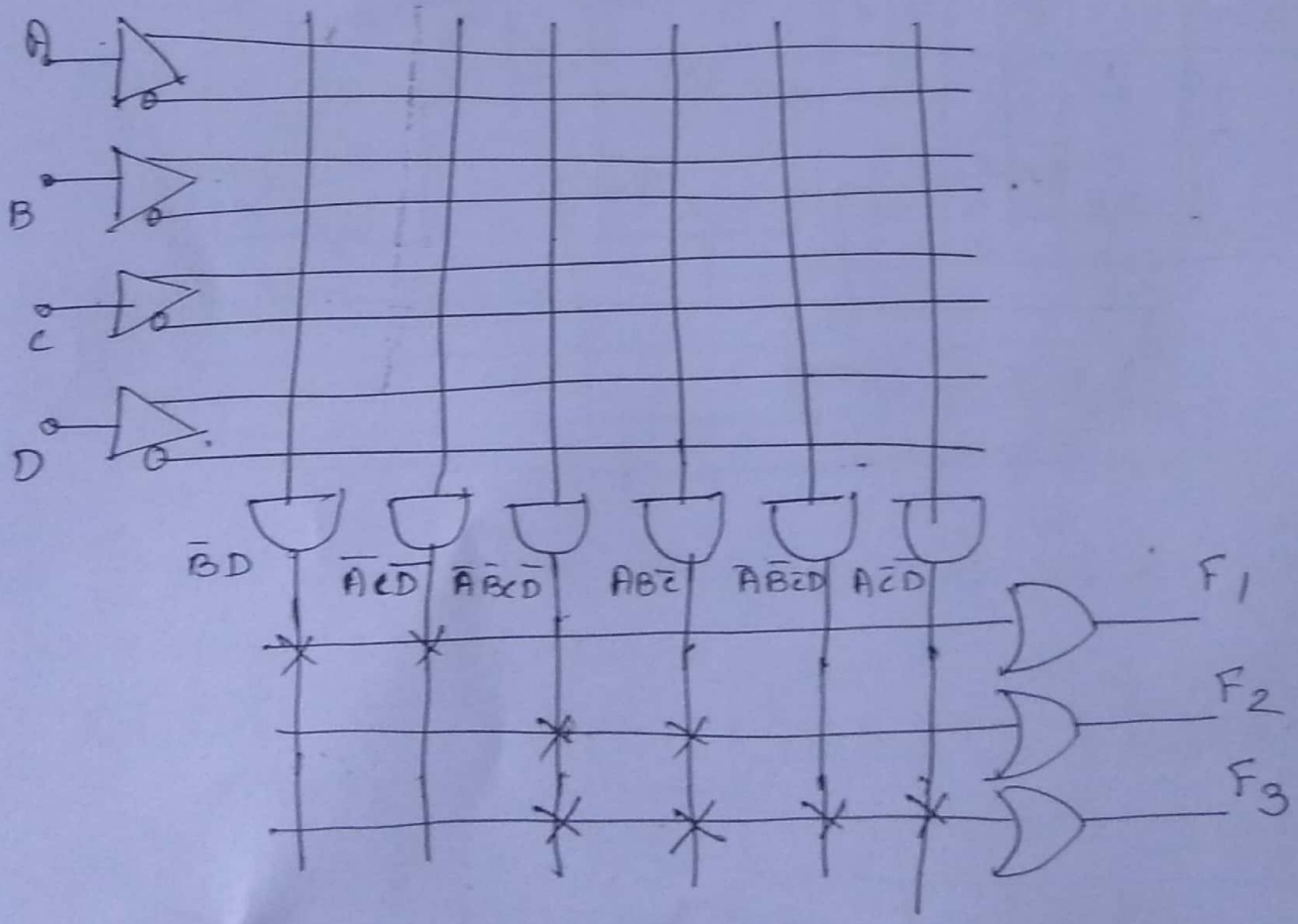
F_2



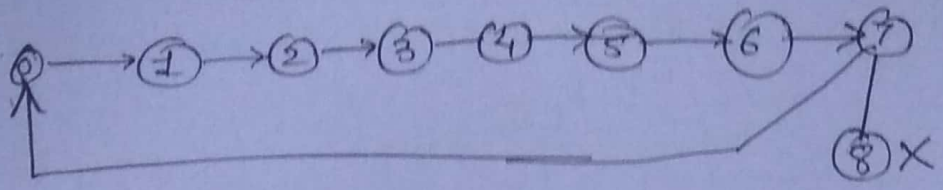
$F_2 = \bar{A}B\bar{C}D + AB\bar{C}$

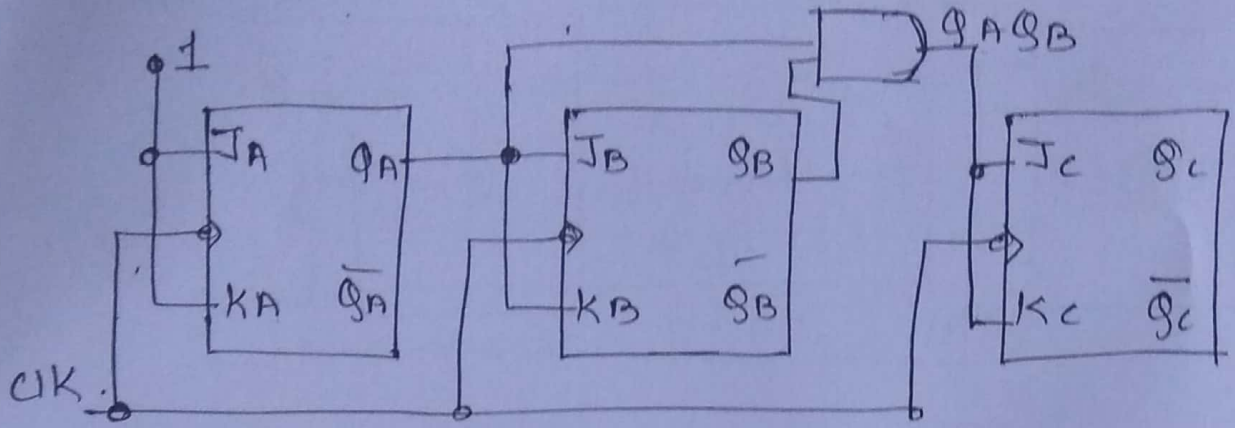


$F_3 = \bar{A}B\bar{C}D + \bar{A}BCD + AB\bar{C} + A\bar{C}\bar{D}$

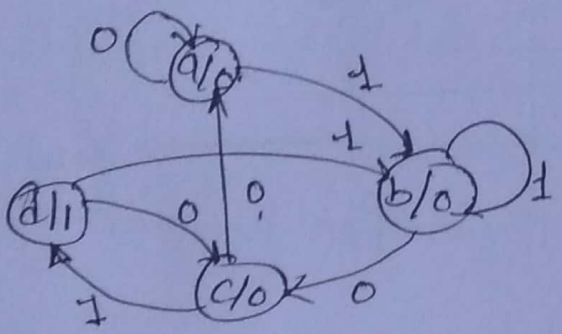


Q4) b) mod-8 binary counter.





Q5) a) 'sequence = '101' using DFF.



P.S.	N.S.		O/P	
	X=0	X=1	X=0	X=01
a	a	b	0	0
b	c	b	0	0
c	a	d	0	1
d	c	b	0	0

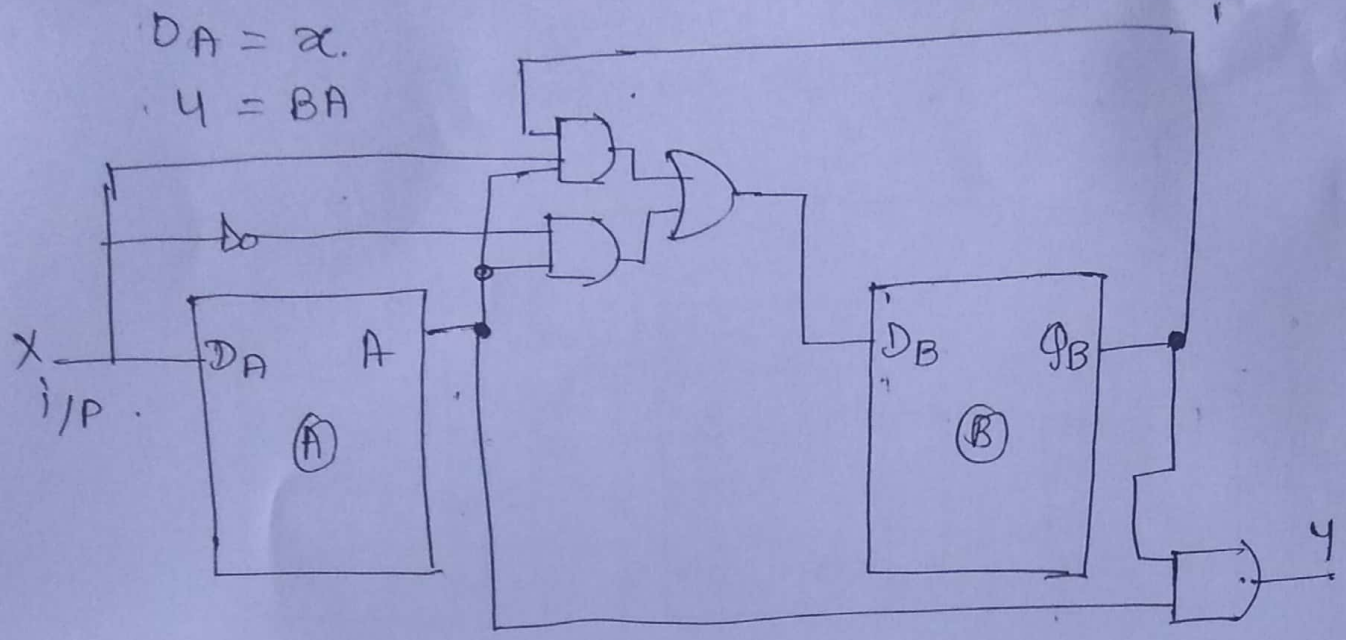
Excitation Table

I/P	P.S.		N.S.		F F I/P.		O/P
x	B	A	B+1	A+1	D_B	D_A	y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	1	0	1	0	1	0
1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	1

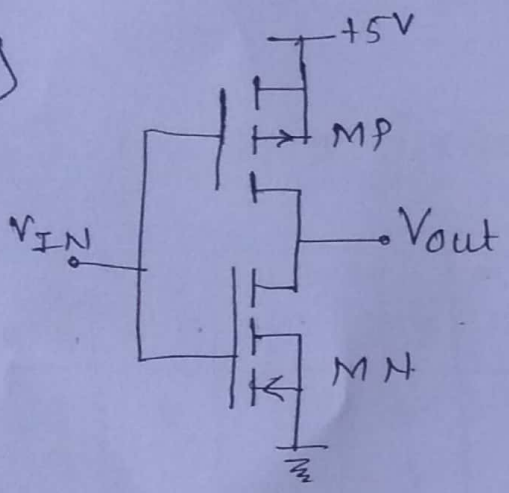
$D_B = \bar{x}A + xBA$

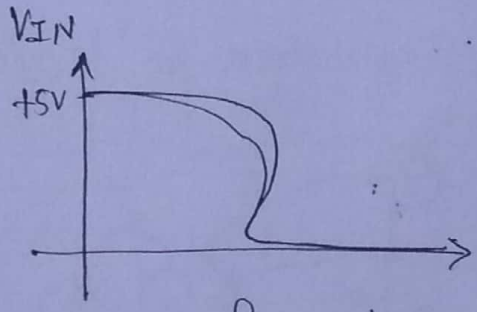
$D_A = x.$

$Y = BA$



Q5) a)



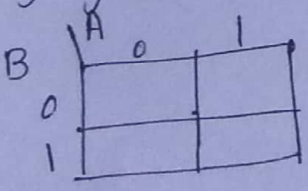


∴ Tuzans fer characteristics.

Q6 a) **K map**

K-map is a graphical method of simplifying a boolean eqn. K-map is a geaphical chart which contains boxes. K-maps can be written for 2,3,4 upto 6 variables.

eg. four. 2 i/p K-map

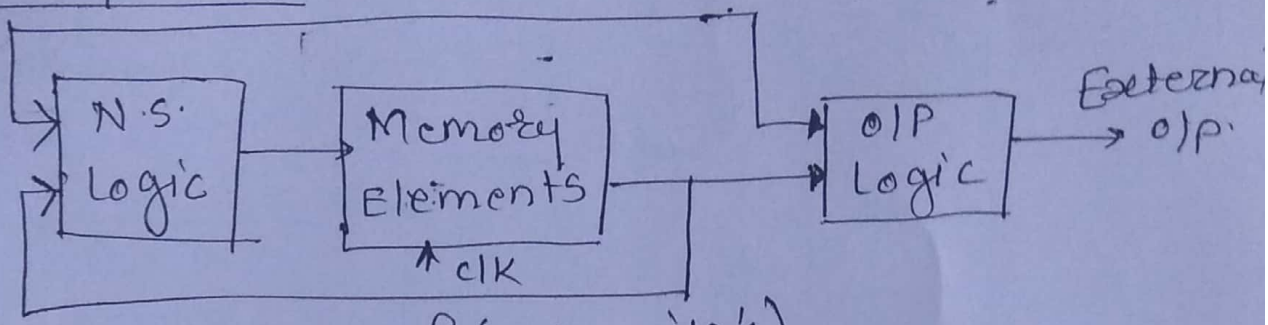


K-map four 2 i/p variable consist of $2^2 = 4$ boxes. Inside these boxes we have to enter the values of o/p Y four diff. combinations of i/p A & B. We can group these values to minimise these Kmap.

Q6 b) Mealy & Moore seq. Machine

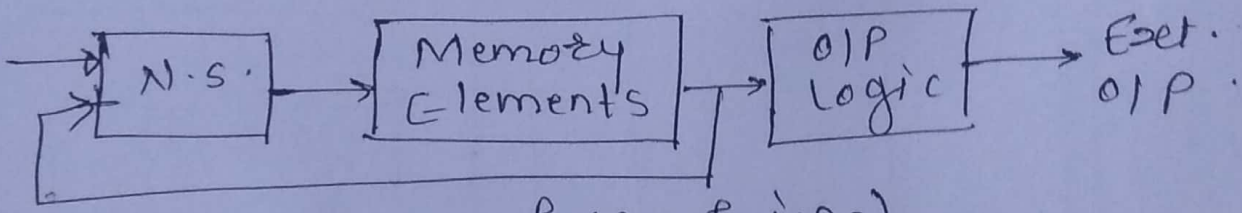
There are two sequential logic design models.

Mealy Model



N.S. = O/P = f(P.S., i/p's)

Moore Model



N.S. = f(P.S & i/ps)

O/P = f.(P.S.)

Q6 d) XC9500 family.

XC9500 CPLD is xilinx architecture. Internal PLD's in xilinx are called as functional blocks. Each PLD has 36 i/p's & 18 microcells & O/P's.

- Here I/O pins can be used as i/p, o/p. or bidirectional i/p.

Here, GCK → Global clock

GSR → Global Set/Reset

GTS → Global three state control.

In diag, there are four FB's. Instead we can use upto 16 FBS, where each FB will receive 36 signals from switch matrix.

XC 9500 diagram