Solution Opcode: 27284

SE/ Sem III / INST/ Digital Electronics/
DEC – 2017 Solution ①

1) a) i) $(FFFA)_{16} = (1111\ 1111\ 1111\ 1010)_2$

$(1\ 7\ 7\ 7\ 7\ 2)_8$

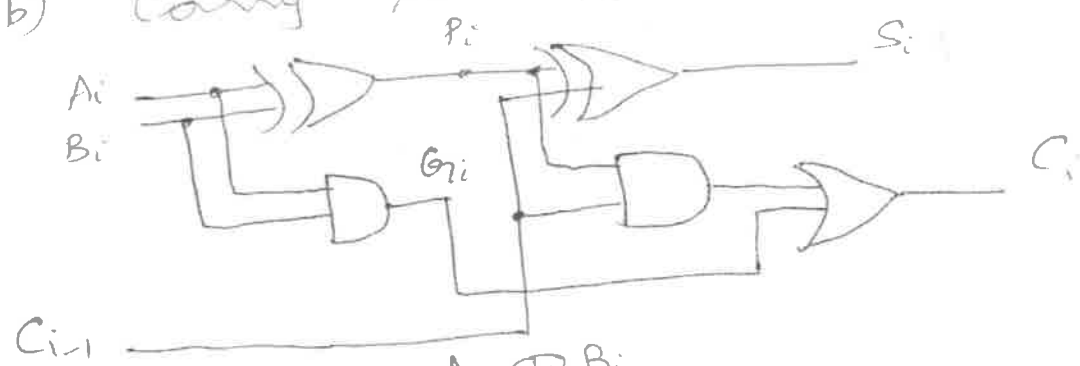
(ii) $(101.1101)_2 = 1\times2^2 + 1\times2^0 + 1\times2^{-1} + 1\times2^{-2} + 1\times2^{-4}$

$= 4 + 1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{16}$

$= 5 + \frac{13}{16}$

$= (5.8125)_{10}$

b) Carry look ahead adder:



$P_i = A_i \oplus B_i$

$G_i = A_i B_i$

$S_i = P_i \oplus C_{i-1} = A_i \oplus B_i \oplus C_{i-1}$

$C_i = G_i + P_i C_{i-1}$

$i=0, \quad P_0 = A_0 \oplus B_0, \quad G_0 = A_0 B_0$

$C_0 = G_0 + P_0 C_{-1}$

$C_1 = G_1 + P_1 G_0 + P_1 P_0 C_{-1}$

$C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{-1}$

$C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{-1}$

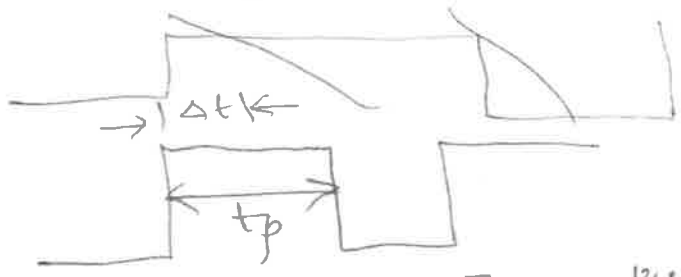
c)

Combinational	Sequential (2)
① output depends upon present input conditions only.	① Output depends not only on present, but also on past conditions.
② No memory	② Memory is required
③ No need for clock pulses	③ clock pulses necessary for synchronization
④ Not So complex	④ complex circuitry
⑤ Ex: Full adder, subtractor, Multiplexer, decoder, etc	⑤ Ex: Flip-flop, counter, register, etc

d) Race - Around Condition:

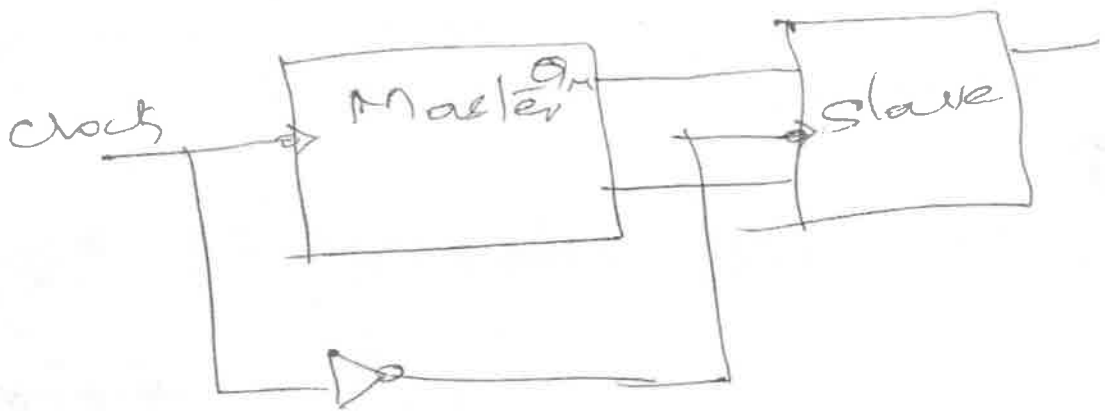
In JK flipflop, when J=K=1, output is $\overline{Q_n}$ i.e. complementary of previous output. Hence during the entire pulse duration, output keeps ontoggling between 0 and 1.

this is occuring since duration of clock pulse tp is of the order of milliseconds, whereas Δt → propagation delay time of Nand gates is of the order of μs



tp → clock pulse duration
Δt → propagation delay time

① This can be avoided if ③ $t_p < \Delta t < T$.
→ very difficult to satisfy because of very small propagation delays in ICs.
② use of Master_slave JK flip flop to avoid this.



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2)a) Hamming code for BCD 0110.

i)

Position	1	2	3	4	5	6	7
	P_1	P_2	n_1	P_3	n_2	n_3	n_4
original BCD			0		1	1	0

Even parity in positions 1,3,5,7 requires $P_1 010 \Rightarrow P_1 = 1$

Even parity in positions 2,3,6,7 requires $P_2 010 \Rightarrow P_2 = 1$

Even parity in positions 4,5,6,7 requires $P_3 110 \Rightarrow P_3 = 0$

∴ Hamming code is

1100110

ii) $A\left[B + C\left(\overline{\bar{A}B + \bar{A}C}\right)\right] = A\left[B + C\left(\bar{A}\bar{B} \cdot \bar{A}\bar{C}\right)\right]$

$= A\left[B + C\,(\bar{A}+\bar{B})(\bar{A}+\bar{C})\right]$

$= A\left[B + C\left(\bar{A} + \bar{A}\bar{C} + \bar{A}\bar{B} + \bar{B}\bar{C}\right)\right]$

$= A\left[B + \bar{A}C + \bar{A}\bar{B}C\right]$

$= AB$

a) ii) b) $\overline{AB \cdot (\overline{C+D}) \cdot AB}$

$= \overline{AB \cdot (\overline{C+D})} = \overline{AB} + \overline{\overline{C+D}}$

$= \overline{AB} + C + D$

$= \bar{A} + \bar{B} + C + D$

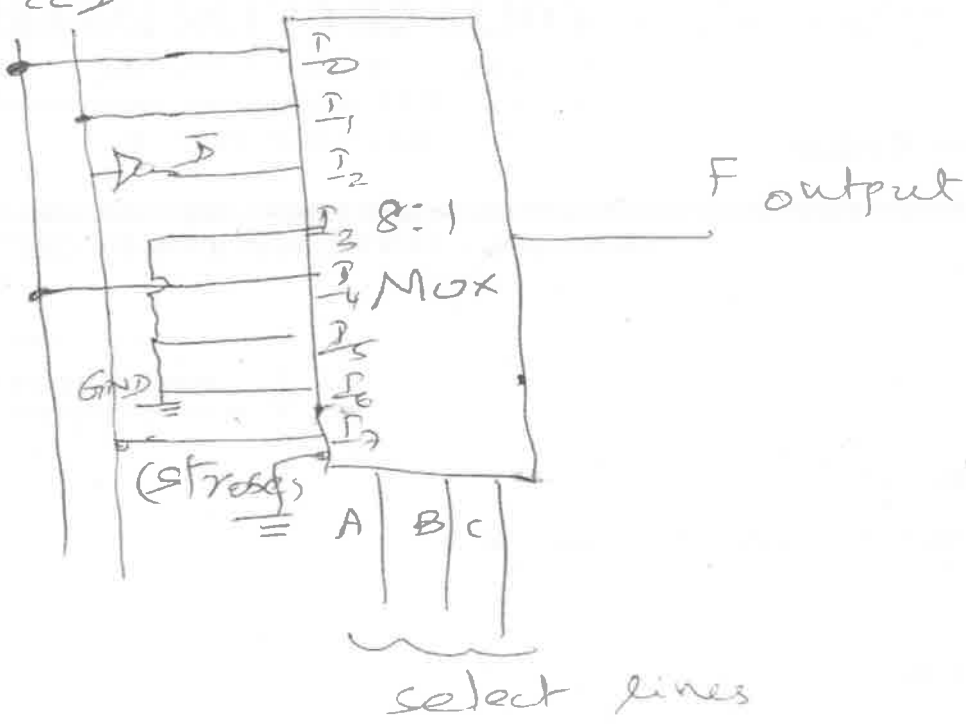
a)b) $F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 8, 9, 15)$

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

→

A	B	C	F
0	0	0	1
0	0	1	D
0	1	0	$\bar{D}$
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	D

2) b) V_{cc} D



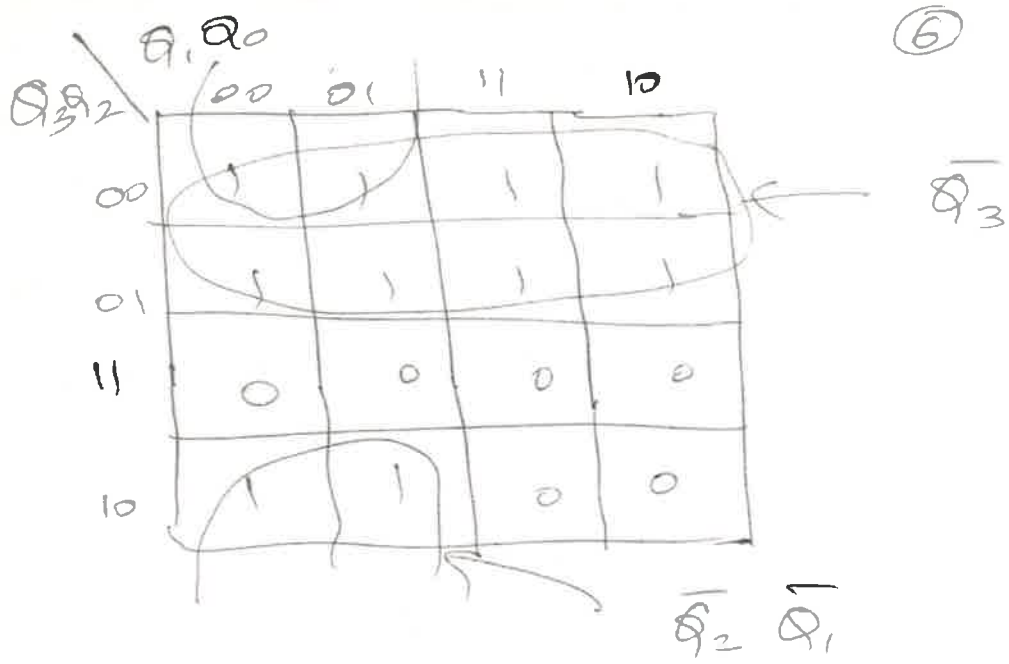
3) a) Decade Ripple counter

Q_3 Q_2 Q_1 Q_0	Output of Reset logic
0 0 0 0	1
0 0 0 1	1
0 0 1 0	1
0 0 1 1	1
0 1 0 0	1
0 1 0 1	1
0 1 1 0	1
0 1 1 1	1
1 0 0 0	1
1 0 0 1	1
1 0 1 0	0
1 0 1 1	0
1 1 0 0	0
1 1 0 1	0
1 1 1 0	0
1 1 1 1	0

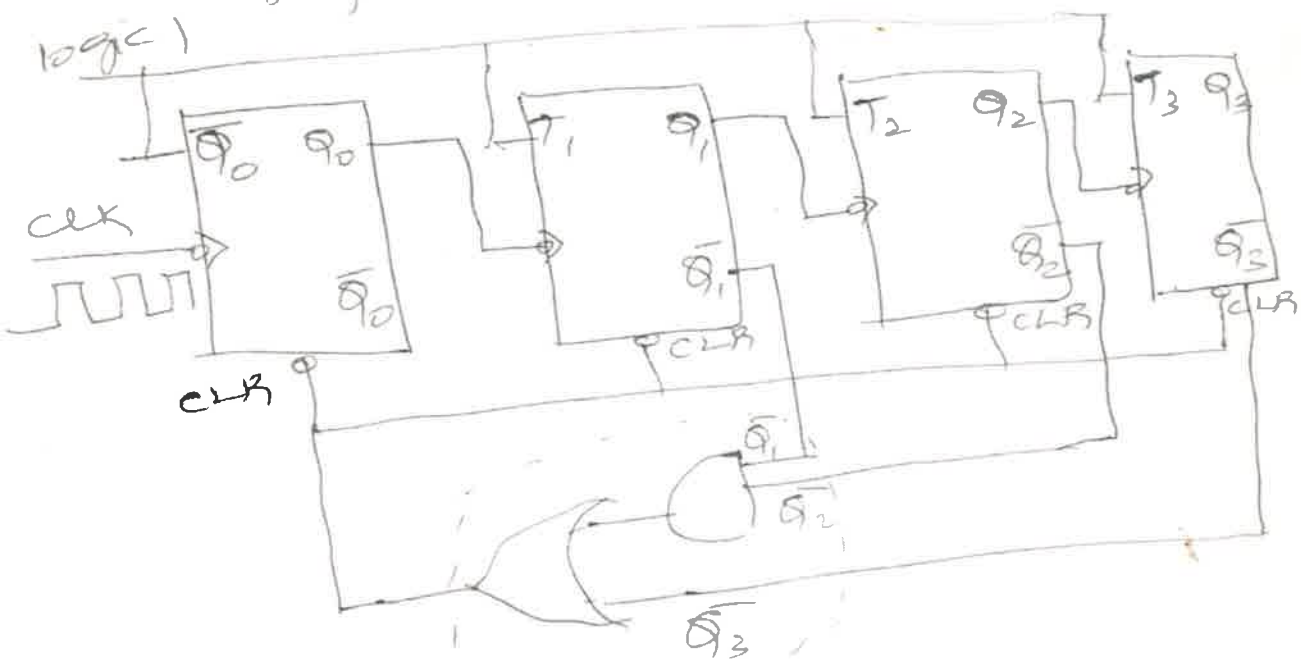
D assign of Reset logic

← Valid states

← Invalid states



o/p of Reset logic = $\bar{Q}_3 + \bar{Q}_2\bar{Q}_1$



Final o/ps from $Q_3Q_2Q_1Q_0$

3) b) Conversion of JK to T Flip flop

Inputs		Transition	output	
Q	T	(i)	J	K
0	0	0	0	X
0	1	1	1	X
1	0	01	X	0
1	1	0	X	1

K-Map for J

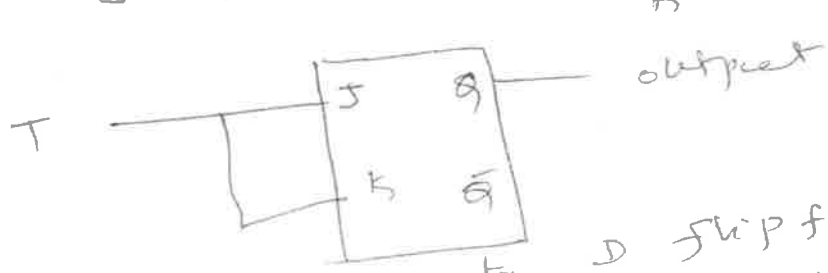
Q \ T	0	1
0	0	1
1	X	X

J = T

K Map for K

Q \ T	0	1
0	X	X
1	0	1

K = T



Conversion of JK to D flip flop

Inputs		Transition	outputs	
Q	D	(i)	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

J

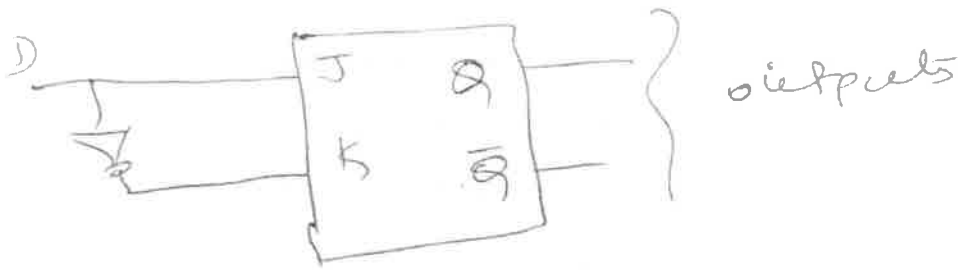
Q \ D	0	1
0	0	1
1	X	X

J = D

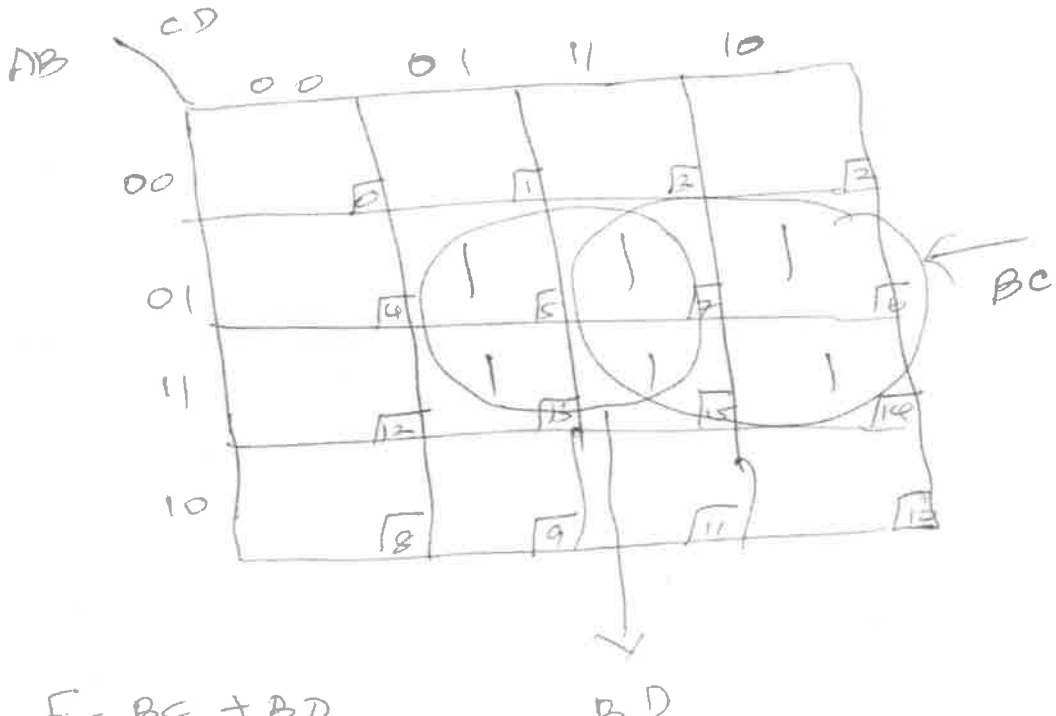
K

Q \ D	0	1
0	X	X
1	1	0

K = D̄



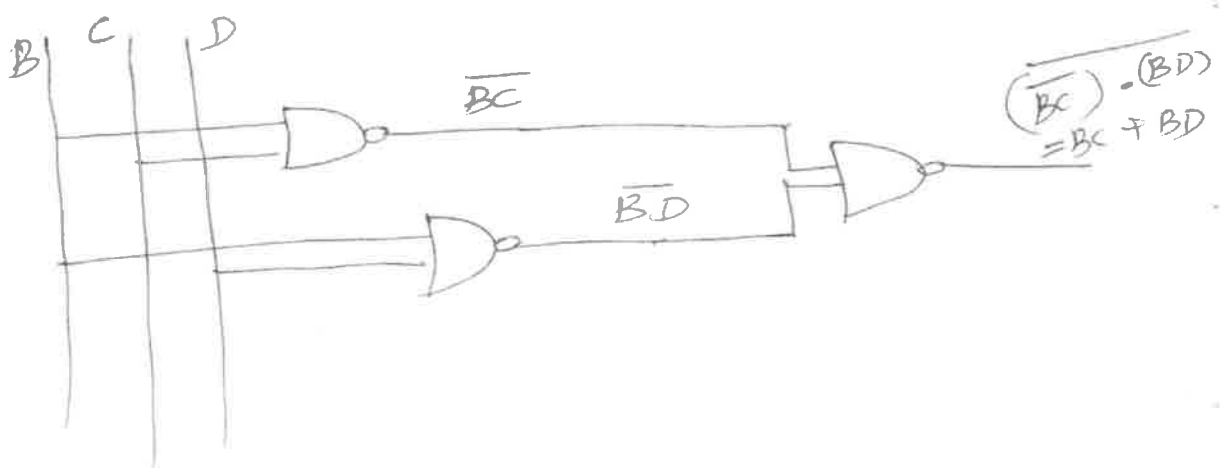
4) a) $F = \sum m(3, 6, 7, 13, 14, 15)$



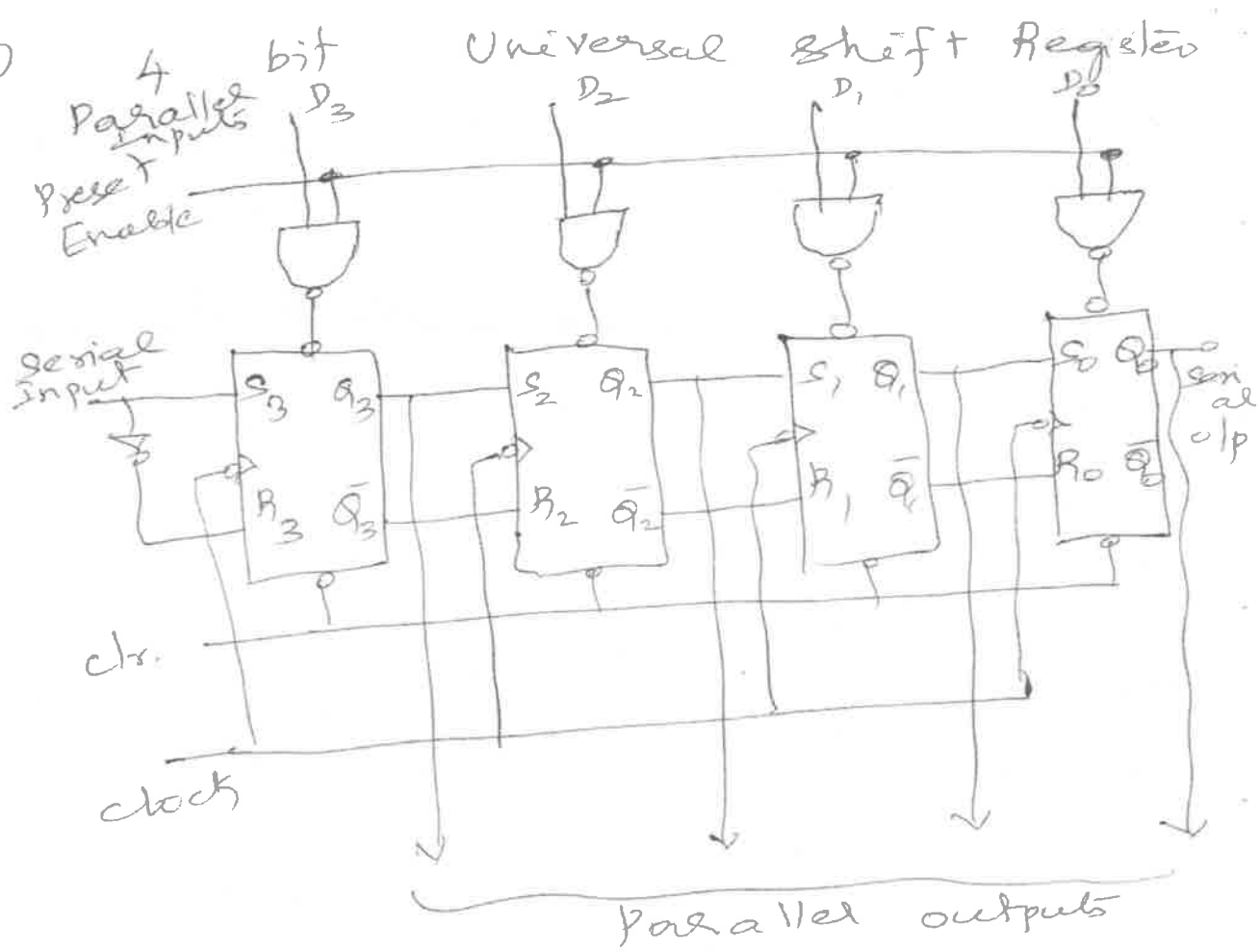
$F = BC + BD$

$\overline{\overline{F}} = \overline{\overline{BC} + \overline{BD}}$

$= \overline{(\overline{BC}) \cdot (\overline{BD})}$



4) b)



SISO, SIPO, PIPO, PISO → all 4 operations possible

Parallel input → I is applied at $\overline{\text{Preset}}$ inputs, whatever data entering through D_3 D_2 D_1 D_0 will be written into the register.