(1)

gp code = 21793

## Model Solution

| Q.1 | | Attempt any 4 questions: | |
|---|---|---|---|
| | (c) | Find $v_N$, $v_P$, and $v_O$ in the circuit of Fig. 1(c) if $v_S$ is 9 V. | [05] |

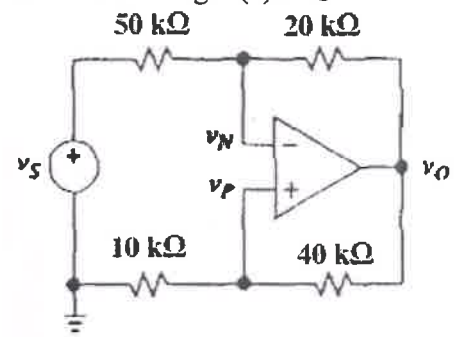


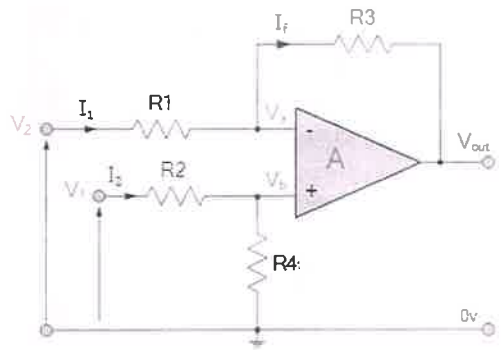

**Fig. 1(c)**

$v_N = v_P = [10/(10+40)]v_O = 0.2v_O$

$(v_S - v_N)/50 = (v_N - v_O)/20 = (9 - 0.2v_O)/50 = (0.2v_O - v_O)/20$

$v_O = -5$ V, $v_N = v_P = -1$ V.

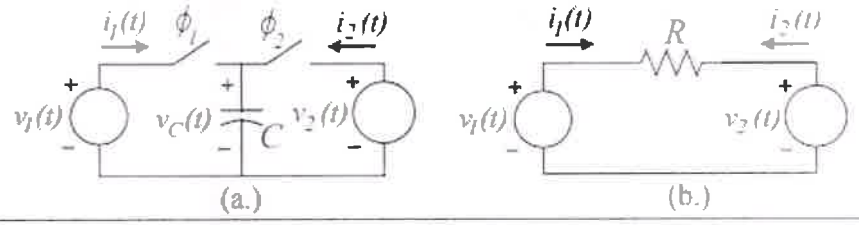
| | (d) | Design a circuit for $V_O = 2V_1 - 3V_2$ using single op-amp and few resistors. | [05] |
|---|---|---|---|



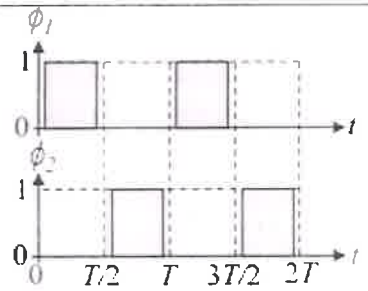

$$V_{out} = -V_2\left(\frac{R_3}{R_1}\right) + V_1\left(\frac{R_4}{R_2+R_4}\right)\left(\frac{R_1+R_3}{R_1}\right)$$

Therefore, R2=R4 and R3=3R1

| | (e) | Explain how a resistor can be simulated by a switch capacitor circuit. | [05] |
|---|---|---|---|



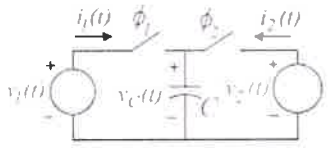
Q 2




Assume that $v_1(t)$ and $v_2(t)$ are changing slowly with respect to the clock period

The average current is,

$$i_1(average) = \frac{1}{T}\int_0^T i_1(t)dt = \frac{1}{T}\int_0^{T/2} i_1(t)dt$$




Charge and current are related as,

$$i_1(t) = \frac{dq_1(t)}{dt}$$

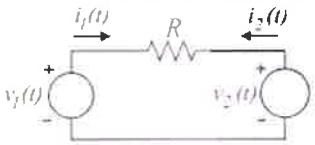
Substituting this in the above gives,

$$i_1(average) = \frac{1}{T}\int_0^{T/2} dq_1(t) = \frac{q_1(T/2)-q_1(0)}{T} = \frac{Cv_c(T/2)-Cv_c(0)}{T}$$

However, $v_C(T/2) = v_1(T/2)$ and $v_C(0) = v_2(0)$. Therefore,

$$i_1(average) = \frac{C[v_1(T/2)-v_2(0)]}{T} = \frac{C[V_1-V_2]}{T}$$

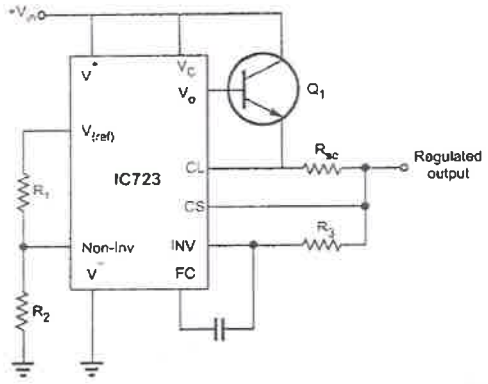
For the continuous time circuit:




$$\Rightarrow i_1(average) = \frac{V_1-V_2}{R} \quad \therefore \quad \boxed{R = \frac{T}{C}}$$

For $v_1(t) = V_1$ and $v_2(t) = V_2$, the signal frequency must be much less than $f_c$

| | | | |
|---|---|---|---|
| Q.2 | (a) | Design a voltage regulator using IC 723 to give $V_o$ = 4 V to 32 V and output current of 2 A.<br>Design a circuit of either low voltage regulator as shown in figure so as to get fixed 4 V output (or high voltage regulator so as to get fixed 32 V output). Then, derive the components for high voltage regulator to vary the voltage from 4 V to 32 V (or derive the components for low voltage regulator to vary the voltage from 4 V to 32 V). | [10] |



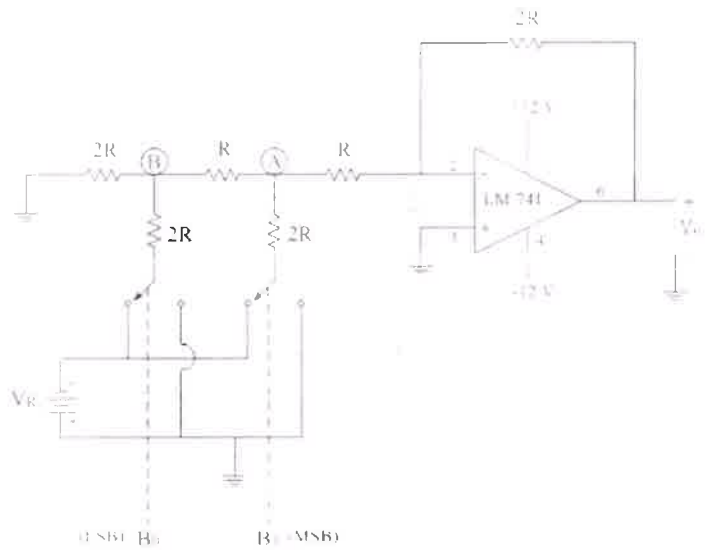

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

$$R_{sc} = \frac{0.6}{I_{limit}}$$

Transistor of appropriate value of β is connected externally, shown as $Q_1$ so as to boost the current to 2 A. Without $Q_1$, the load current will be around 150 mA.

Q3

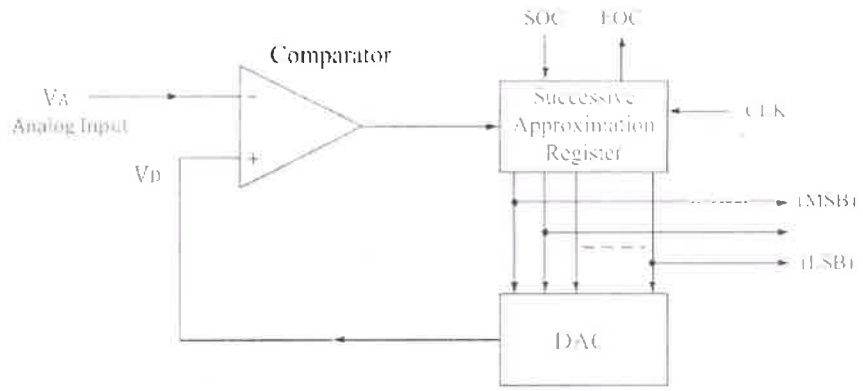
| | | | |
|---|---|---|---|
| | (b) | Explain *R*-2*R* ladder type digital to analog convertor. | [10] |




$$V_o = -V_R \frac{R_f}{R}\left[\frac{B_1}{2^1} + \frac{B_0}{2^2} + \frac{B_{-1}}{2^3} + \cdots\cdots + \frac{B_{-n}}{2^{n+1}}\right]$$

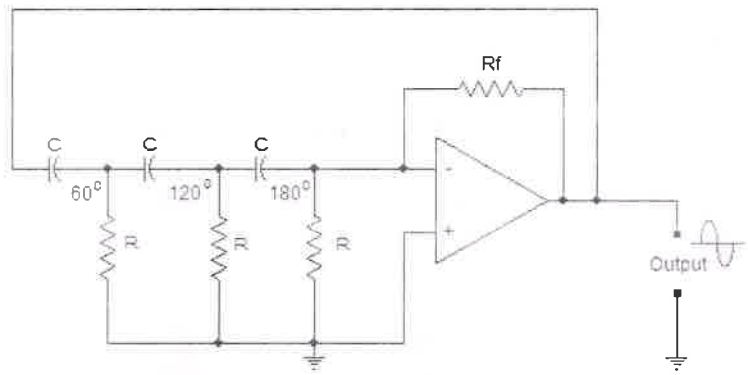
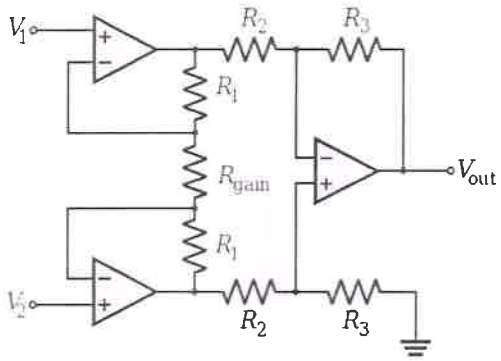
| Sr. No. | Digital Input | | Analog Output, $V_o$(V) |
|---|---|---|---|
| | $B_1$ | $B_0$ | |
| 01 | 0 | 0 | 0 |
| 02 | 0 | 1 | $\frac{V_R}{4}$ |
| 03 | 1 | 0 | $\frac{2V_R}{4}$ |
| 04 | 1 | 1 | $\frac{3V_R}{4}$ |

| | | | |
|---|---|---|---|
| Q.3 | (a) | Explain analog to digital conversion using successive approximation method. | [10] |

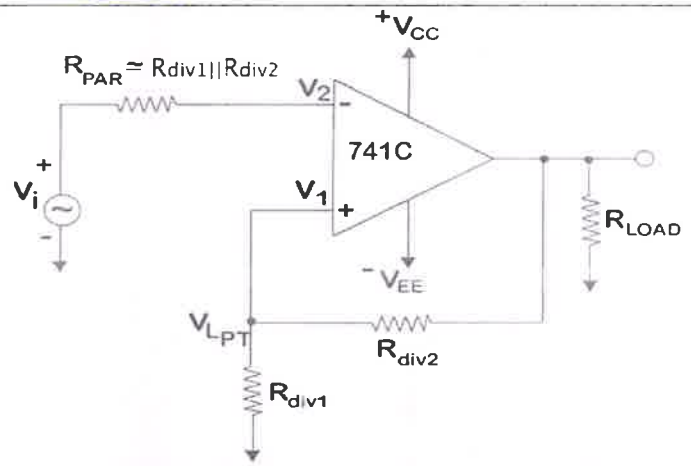



Explanation of Successive approximation type ADC.

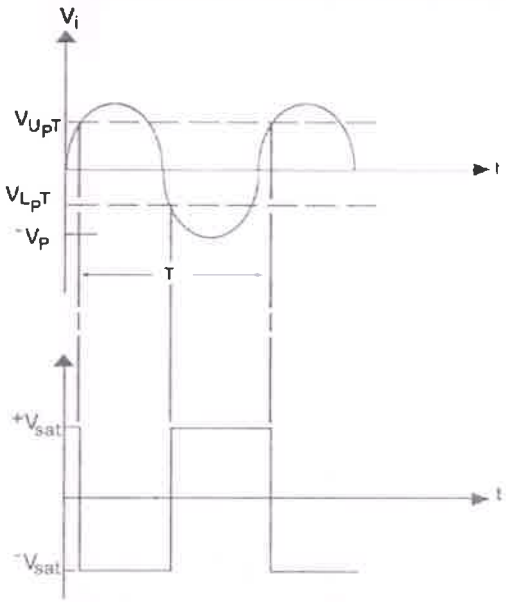
04

| | | | |
|---|---|---|---|
| | (b) | Draw a neat circuit diagram of a *RC* phase shift oscillator using op-amp. Derive its frequency of oscillation. What are the values of *R* and *C* for frequency of oscillation to be 1 kHz?<br>  <br><br>RC Phase shift oscillator using opamp<br>Derive:<br>$f_o = \frac{1}{2\pi(\sqrt{6})CR}$<br>Choose *C* to derive *R* for $f_o$= 1 kHz. | [10] |
| Q.4 | (a) | What is an instrumentation amplifier? Draw a neat circuit of an instrumentation amplifier using 3 op-amps. Derive its output voltage equation.<br>An instrumentation amplifier is a type of differential amplifier that has been outfitted with input buffer amplifiers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment.<br>  <br><br>$\frac{V_{out}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{gain}}\right)\frac{R_3}{R_2}$<br>Derivation of $V_{out}$. | [10] |
| | (b) | With the help of a neat diagram and voltage transfer characteristics explain the working of an inverting Schmitt trigger. Derive the expressions for its threshold levels. | [10] |

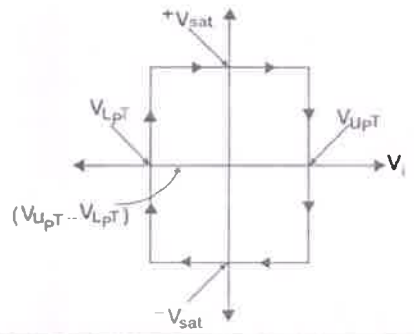
05




SCHMITT TRIGGER - INPUT AND OUTPUT WAVEFORM



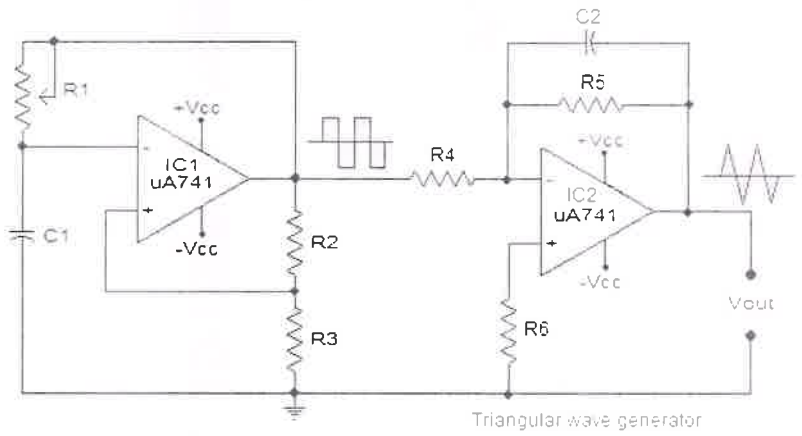

SCHMITT TRIGGER - INPUT OUTPUT CHARECTERISTICS-
HYSTERISIS VOLTAGE PLOT




| | | | |
|---|---|---|---|
| Q.5 | (a) | Draw the circuit diagram of a square and triangular waveform generator using op-amp and explain its working with the help of waveforms.<br><br>Initially, when power is not applied the voltage across the capacitor C1 is 0. When the power supply is switched ON, the C1 starts charging through the resistor R1 and the output of the opamp will be high (+Vcc). A fraction of this | [10] |

06

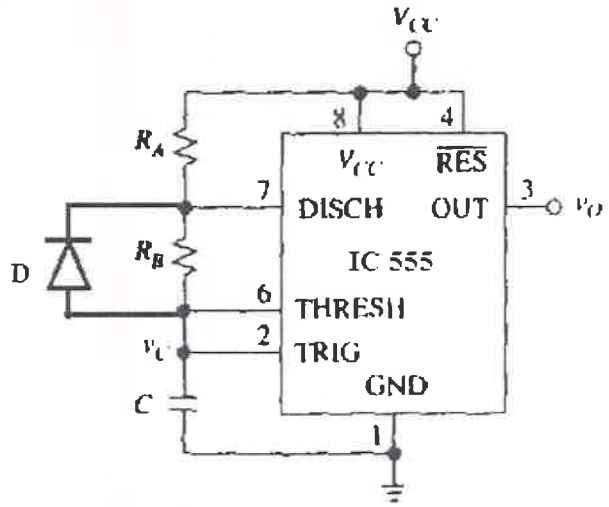
high voltage is fed back to the non- inverting pin by the resistor network R2, R3. When the voltage across the charging capacitor is increased to a point the the voltage at the inverting pin is higher than the non-inverting pin, the output of the opamp swings to negative saturation (-Vcc). The capacitor quickly discharges through R1 and starts charging in the negative direction again through R1. Now a fraction of the negative high output (-Vcc) is fed back to the non-inverting pin by the feedback network R2, R3. When the voltage across the capacitor has become so negative that the voltage at the inverting pin is less than the voltage at the non-inverting pin, the output of the opamp swings back to the positive saturation. Now the capacitor discharges trough R1 and starts charging in positive direction. This cycle is repeated over time and the result is a square wave swinging between +Vcc and -Vcc at the output of the opamp.



Triangular wave generator

If the values of R2 and R3 are made equal, then the frequency of the square wave can be expressed using the following equation: ***F=1 / (2.1976 R1C1)***

(b) Analyze the circuit given in Fig. 5(b). Draw the waveforms at output terminal $v_O$ and across the capacitor $C$. Comment on the duty cycle of output waveform. Take diode D as an ideal diode and assume $R_A$ is equal to $R_B$. [10]



07

**Fig. 5(b)**

The circuit is basically in astable multivibrator mode. Here, while charging the capacitor, capacitor charges through RA and RB (since diode D is connected reverse). Thus, $Tc = 0.694(R_A+R_B)*C$. While discharging, the capacitor will discharge through diode D (since diode D is ideal, offers zero resistance). Thus. $T_d = 0.694\ R_D*C = 0$. Therefore, Duty cycle= $T_c/(T_c+T_d)$=100% (approximately) provided ON resistance of internal transistor connected to discharge pin 7 is zero.)

*******