model solution. Gp code :- 25072

N.B. : (1) Question No. 1 is compulsory.

(2) Solve any three questions from the remaining five

(3) Figures to the right indicate full marks

(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt any 5 questions [20]

a) Prove that for a JFET the gate-source bias for zero temperature drift of drain current is at $|V_P| - 0.63$ volts.

b) Explain the hybrid pi model of BJT.

c) Explain Zener as voltage regulator.

d) Consider a BJT has parameters f_T =500MHz at I_C = 1mA, β = 100 and $C\mu$ = 0.3pF. Calculate bandwidth of f_β and capacitance $C\pi$ of a BJT.

DATA :-

f_T (cut off freq) = 500MHz

I_C = 1mA

β = 100

C_μ = 0.3 pF

TO FIND :-

f_β = ?

C_π = ?

SOLUTION :

STEP 1 $f_\beta = \frac{f_T}{\beta} = \frac{500 \times 10^6}{100} = 5MHz$

$f_\beta = 5MHz$

STEP 2 :

$g_m = \frac{I_C}{V_T} = \frac{1 \times 10^{-3}}{26 \times 10^{-3}}$

$= 38.5 \text{ mA/V}$

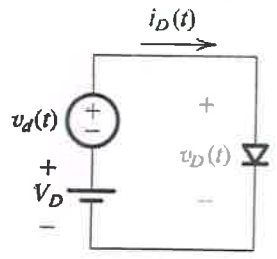
STEP 3 :

$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$

$500 \times 10^6 = \frac{38.5 \times 10^{-3}}{2\pi(C_\pi + 0.3 \times 10^{-12})}$

$C_\pi = 12pF$

e) Draw and explain small signal model of a diode.



Q 2

f) Why should R_C be as large as possible in the design of CE amplifier?

Q.2 a) Design a voltage divider bias network using a supply of 24 V, a transistor with β=110 and an operating point of I_{CQ} = 4 mA and V_{CEQ} = 8V. [10]

Assume $V_E = \frac{1}{8}V_{CC}$.

STEP 1 : KVL to o/p loop.

$V_{CC} - I_C R_C - V_{CE} - V_E = 0$

$R_C = 3.25\,k\Omega$

STEP 2 : $V_E = I_E R_E$

$R_E = 750\Omega$

STEP 3 :

$V_{th} - I_B \times R_{th} - V_{BE} - V_E = 0$

$V_{th} = \frac{R_2}{R_1+R_2} \times 24$

$R_{th} = \frac{R_1 R_2}{R_1+R_2}$

$V_{th} = \frac{R_{th}}{R_1} \times 24 \Rightarrow R_{th} = \frac{V_{th} \times R_1}{24}$

Let $R_1 = 10k$

$V_{th} = 3.756\ V$

$R_{th} = \frac{3.756 \times 10k}{24}$

$R_{th} = 1.565\,k$

$R_{th} = \frac{10k \times R_2}{10k + R_2}$

$R_2 = 1.855k$

b) Explain the fabrication steps of passive elements. [5]

Fabrication Steps are:

Silicon Wafer preparation, Epitaxial Growth, Oxidation, Diffusion, Ion implantation, Isolation technique, Metallization, Assembly processing and packaging.

Q3

c) What are the important JFET parameters and define it from characteristics. [5]

Drain resistance rd = $\Delta V_{DS} / \Delta I_D$
Tran conductance gm= $\Delta I_D / \Delta V_{GS}$
Amplification factor $\mu = \Delta V_{DS} / \Delta V_{GS} = (\Delta V_{DS} / \Delta I_D) \text{ X } (\Delta I_D / \Delta V_{GS}) = \text{rd X gm}$

Q.3 a) Design the resistors of a single stage CS amplifier for audio frequency with BFW11 with $I_{DS} = (3.3 \pm 0.6)\text{mA}$ and $|A_V| = 12$. [10]

STEP 1 : DATA FROM DATASHEET

I_{DSS} - 7mA, g_{mo} = 5600 μ℧, V_P = -2.5V, rd = 50k

STEP 2 : SELECTION OF BIASING TECHNIQUE

Since variation in parameter is given, we will select potential divider biasing.

STEP 3 : CALCULATION FROM GRAPH OF TRANSFER CHARACTERISTICS.

(OBSERVATION TABLE FOR GRAPH TO BE TAKEN FROM DATASHEET MENTIONED AS JFET MUTUAL CHARACTERISTICS.

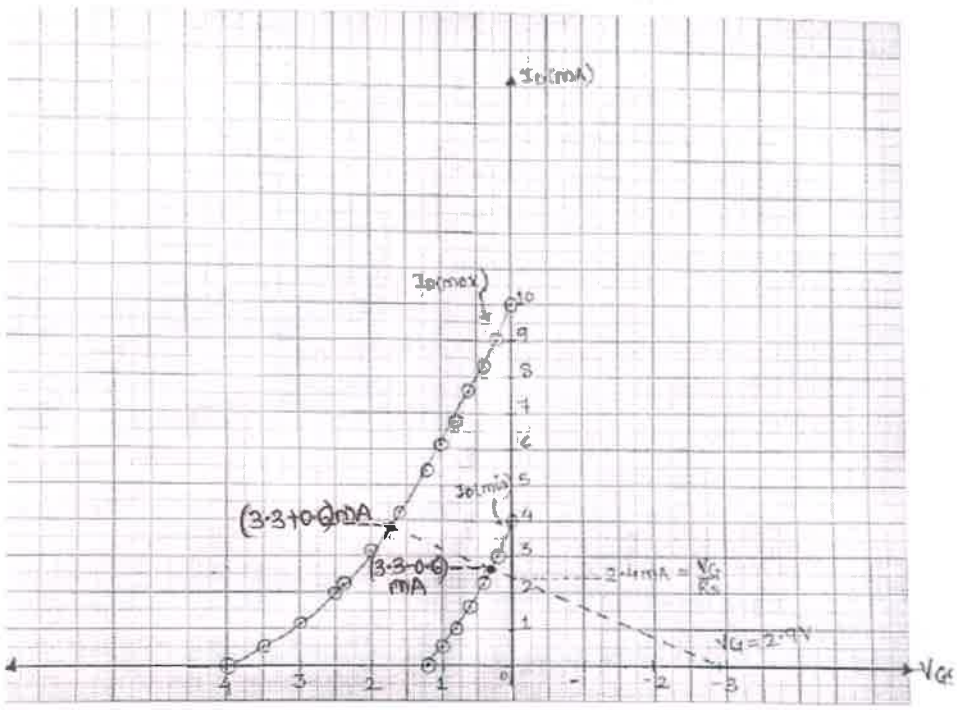
From graph $V_G = 2.9V$ and $\frac{V_G}{R_S} = 2.4\text{mA}$

$\therefore R_S = \frac{V_G}{2.4\text{mA}} = \frac{2.9}{2.4 \times 10^{-3}} = 1.208\text{k}\Omega$

Let $R_S = 1.2\text{k}\Omega / \frac{1}{4}\text{W}$

$V_{GSQ} = V_G - I_{DQ} R_S$.

$I_{DQ} = \frac{I_{D(max)} + I_{D(min)}}{2} = \frac{3.9\text{m} + 2.7\text{m}}{2} = 3.3\text{mA}$



04

STEP 5: CALCULATION OF R_D.

$$|A_V| = g_m (r_d \| R_D)$$

STEP 6: CALCULATION OF V_{DSQ}

since V_O is not given let $V_O = 2V$.

$$\therefore V_{DSQ} = 1.5 [V_{O(P)} + |V_P|]$$

STEP 7: CALCULATION OF V_{DD}

$$V_{DD} = I_{DQ} (R_S + R_D) + V_{DSQ}$$

STEP 8: CALCULATION OF R_1 and R_2

$$V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2}$$

$$\frac{R_1}{R_2} = \frac{V_{DD}}{V_G} - 1.$$

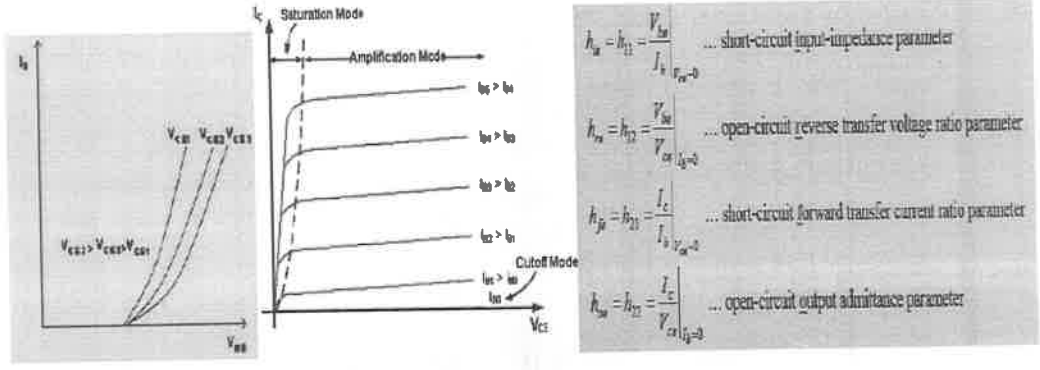
b) Draw CS JFET amplifier with self bias circuit and derive the expression for voltage gain input impedance and output impedance. [10]

i) Circuit Diagram

ii) Small Signal Hybrid Pi model

iii) Derivation of expression of voltage gain, input resistance and output resistance

Q.4 a) Draw small signal hybrid parameter equivalent circuit for CE amplifier and define the same. What are the advantages of h parameters? [10]



Mention advantages of h parameters

b) For the circuit shown below in Fig.4b, the transistor parameters are $V_{BE\,(on)} = 0.7$ V, $\beta = 200$ and $V_A = \infty$. [10]

i) Derive the expression for lower cut-off frequency (or time constant) due to input coupling capacitor.

ii) Determine lower cut-off frequency and midband voltage gain.

05

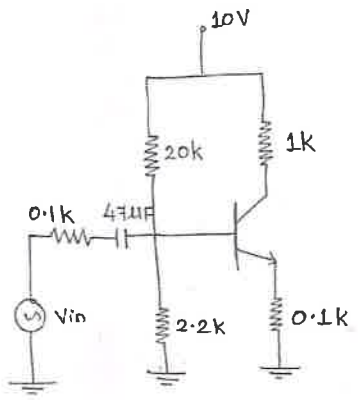


Fig.4b

DC Analysis (calculate g_m and r_π)

AC analysis

Derivation of expression for time constant

$$\tau_s = (R_s + Z_i) \cdot C_C$$

$$f_L = \frac{1}{2\pi\tau_s}$$

$$|A_{V(max)}| = \frac{g_m r_\pi R_C}{(R_s + Z_i)} \times \frac{R_B}{(R_B + Z_b)}$$

Q.5 a) Design an L section LC filter with full wave rectifier to meet the following specifications: The DC output voltage $V_{DC} = 220\,\text{V}$, deliver $I_L = (70 \pm 20)\text{mA}$ to the resistive load and the required ripple factor is 0.04. [10]

Ripple factor $\gamma = \frac{1}{6\sqrt{2}\,\omega^2 LC}$

Critical inductance $L_c = \frac{R_L}{3\omega}$

$$R_L = \frac{V_{o(dc)}}{I_L}$$

Calculate value of L and using formula of ripple factor calculate value of C.

b) For the circuit shown below in Fig.5b, the transistor parameters are $V_{BE\,(on)} = 0.7$ V, $\beta = 100$ and $V_A = \infty$. Determine Z_i, Z_o and A_V [10]

06

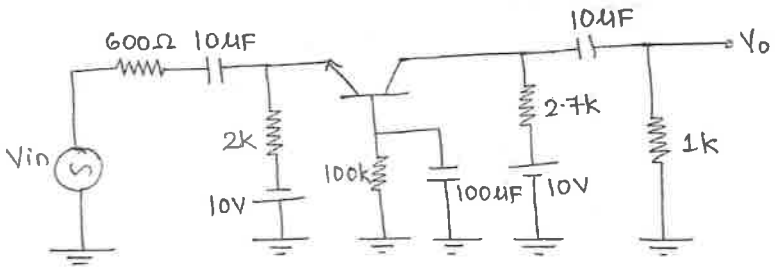
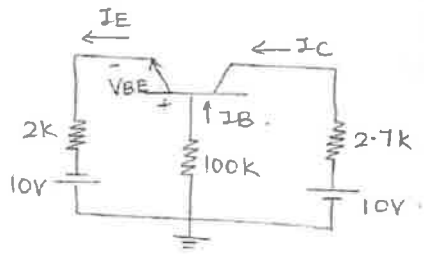


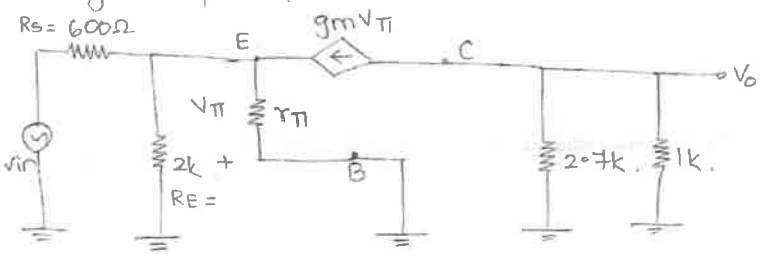
Fig. 5b

STEP 1 : DC ANALYSIS.



STEP 2 : AC ANALYSIS.

Hybrid pi equivalent circuit.



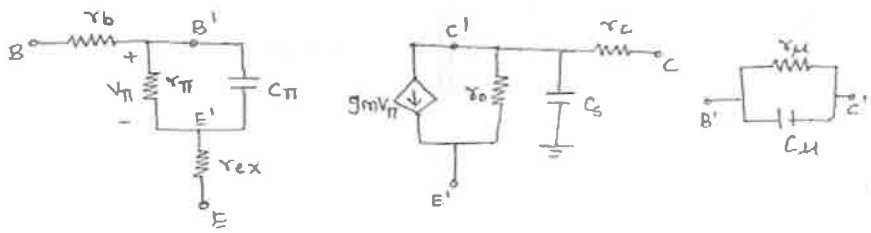
$$V_o = -g_m V_\pi (2{\cdot}7k \| 1k)$$

$$R_i = \frac{r_\pi}{1+\beta}$$

$$R_o = 2{\cdot}7k \| 1K$$

Q.6 Short notes on: (Attempt any four) [20]

a) BJT high frequency equivalent circuit



components of hybrid pi eq. a) Base - emitter b) Collector-emitter c) Base - collector

07

b) Types of resistors and capacitors

-> Resistors are broadly classified into 2 categories

a) Fixed resistors

Symbol : 

→ They are classified as carbon composition, metalized type, wire wound type.

b) Variable or adjustable resistors

-> For circuits requiring a resistance that can be adjusted while it remains connected in the ckt (such as volume control on a radio), variable resistors are required.

→ They have 3 leads, 2 fixed and one movable.

c) Stability factors of various biasing techniques of BJT

Biasing refers to the application of D.C. voltages to setup the operating point in such a way that output signal is undistorted throughout the whole operation. Once selected properly, the Q point should not shift because of change of IC due to β variation due to replacement of the transistor of same type and Temperature variation

The process of making operating point independent of temperature changes or variation in transistor parameters is known as stabilization.

Expression of stability factors of various biasing techniques.

d) Different types of filters
Mention details of L, C, LC, CLC filter.

e) Comparison of BJT CE and JFET CS amplifier
Mention 5 points of comparison.

81.a

$$0.007\, I_D = 0.0022\, g_m$$

$$\frac{I_D}{g_m} = 0.314$$

$$I_D = I_{DSS}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \quad \& \quad g_m = -\frac{2I_{DSS}}{V_p}\left(1 - \frac{V_{GS}}{V_p}\right)$$

$$\frac{\left(1 - \frac{V_{GS}}{V_p}\right) \times V_p}{-2} = 0.314$$

$$|V_p| - |V_{GS}| = 0.63$$

$$\therefore |V_{GS}| = |V_P| - 0.63$$