(1)

QP = 22624

N.B. : (1) Question No. **1** is **compulsory.**

(2) Solve any **three** questions from the remaining **five**

(3) Figures to the right indicate full marks

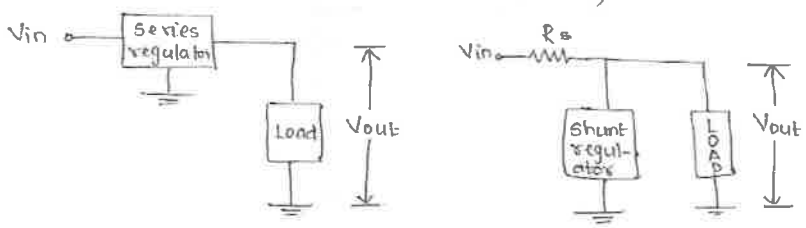
(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt any 5 questions [20]

a) Compare series and shunt regulator.

i) Series vltg regulator (In this the regulating element is placed in series with the load)

ii) Shunt vltg regulator (In this regulating element is placed in parallel with the load)

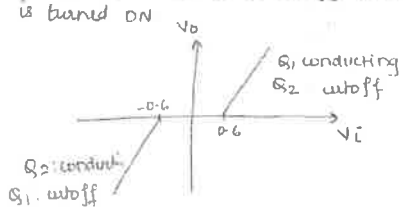


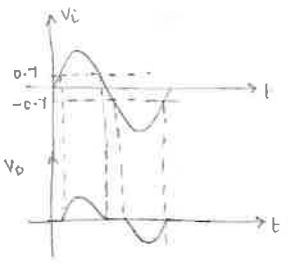
b) What are the major limitation of class B power amplifier and how to overcome the same?

→ In class B power amplifier base current will not flow till ip becomes equal to cut in voltage of transistor.

→ Under this condition, sinusoidal i/p voltage will not produce sinusoidal o/p voltage.

→ o/p voltage is distorted during cross over i.e when one transistor is cutoff and other transistor is turned ON





Remedy to overcome cross over distortion.

→ Cross over distortion can be eliminated by making some changes in existing class B ckt.

→ The change is that a small forward voltage is applied to each transistor to overcome its cut in voltage.

→ Therefore the Q pt is shifted slightly above X axis and the operation is no more a class B but class AB operation.

02

c) What is the need of dual power supply biasing for differential amplifier?
The differential amplifier using discrete devices employs dual power supply. This is to reduce the number of biasing resistors employed when a single power supply is used. When single power supply is used we need two biasing resistors per transistor. This means a total of four resistors can be avoided which results in substantial reduction in the chip area.

d) Which type of biasing technique is used to bias Integrated Circuit

→ The biasing techniques for BJT and FET amplifiers for most part used voltage divider resistor networks

→ This technique can be used for discrete ckts it is not suitable for integrated circuits

→ This is because of fabrication of resistor on IC requires more area as compared to that of transistor. So fabric^{n} of resistor intensive ckt would require a large area.

→ It is also impossible to fabricate capacitors in uF ranges on an IC. So coupling or bypass cap cannot be fabricated on an IC.

→ Hence biasing of transistor circuits in IC is completely different than that in discrete transistor design.

e) Draw and explain frequency response of BJT CE amplifier.

f) Explain line regulation and load regulation of voltage regulator. Draw the line and load regulation characteristics of ideal and practical voltage regulator.

→ The quality of IC regulator is often determined on the basis of three important parameters: line regulation, load regulation and ripple rejection

i) Line regulation : It is dependent on operating temperature of regulator.

→ Lesser line regulation implies better quality of an IC.

→ It is defined as the change in the regulated o/p vltg due to change in unregulated i/p vltg over a specific range.

ii) Load regulation : It describes change of o/p vltg over a specified load current.

→ For eg: LM7815 has load regulation of 12mV. for change of load current over a range from 5mA to 1.5A.

03

Q.2 a) For the circuit shown in Fig. 2a, the transistor parameters are $V_{BE(on)}$ = 0.7V, β=100, C_π = 2 pF, Cμ = 0.2 pF. Find lower cutoff frequency and midband gain. [10]

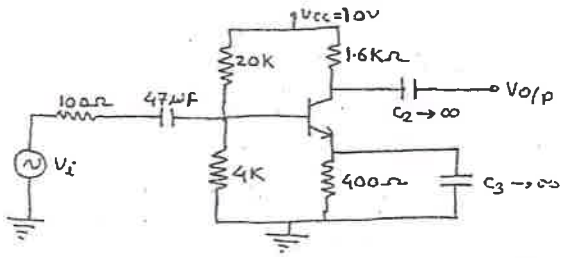
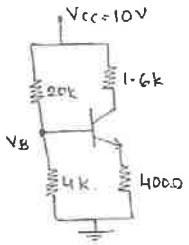


Fig.2a

STEP 1: DC ANALYSIS



$V_B = \frac{4K \times 10}{4K+20K} = 1.667V$

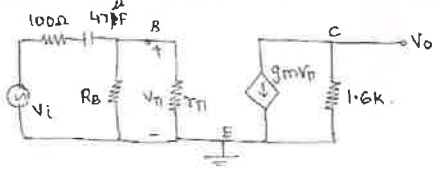
$\therefore I_C \cong I_E = 2.417mA$

$g_m = \frac{I_C}{V_T} = \frac{2.417 \times 10^{-3}}{26 \times 10^{-3}} = 92.9\ mA/V$

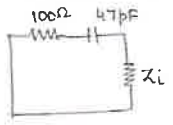
$g_m = \frac{\beta}{r_\pi}$

$\therefore r_\pi = \frac{100}{92.9 \times 10^{-3}} = 1076.426$

STEP 2: AC ANALYSIS [LOW FREQUENCY RESPONSE]



Using time constant technique



where

$Z_i = R_B \| r_\pi$

$= R_1 \| R_2 \| r_\pi$

$= 20k \| 4k \| 1076.426$

$= 813.227\Omega$

$\therefore \tau_S = R_{eq} \times C_{C_1}$

$= (Z_i + R_S) \times C_{C_1}$

$= (813.227 + 100) \times 47 \times 10^{-6}$

$= 0.0429\ sec$

$f_L = \frac{1}{2\pi\tau_S}$

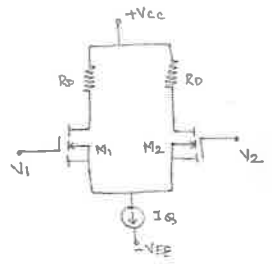
$= \frac{1}{2\pi \times 0.0429}$

$f_L = 3.709\ Hz$

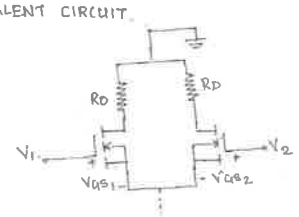
04

b) Determine unity gain bandwidth of N channel MOSFET with parameters $K_n = 0.25\ mA/V^2$, $V_{TN} = 1V$, $\lambda=0$, $C_{gd} = 0.04\ pF$, $C_{gs} = 0.2\ pF$, $V_{GS} = 3V$. If a $10\ k\Omega$ load is connected to the output between drain and source determine the Miller capacitance and cut-off frequency. [10]

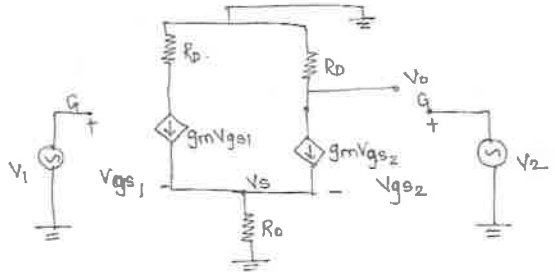
Q.3 a) Draw circuit diagram of MOSFET based differential amplifier and derive the expression for differential gain, common mode gain and CMRR. [10]



AC EQUIVALENT CIRCUIT



DC supply is shorted to ground and current source is assumed to have infinite o/p ree



KCL at node Vs.

$$\frac{V_s}{R_o} = g_m V_{gs_1} + g_m V_{gs_2}$$

$$V_{gs_1} = V_1 - V_s$$

$$V_{gs_2} = V_2 - V_s$$

$$g_m (V_1 - V_s + V_2 - V_s) = \frac{V_s}{R_o}$$

$$g_m R_o (V_1 + V_2) = V_s + 2g_m R_o V_s$$

$$V_s = \frac{g_m R_o (V_1 + V_2)}{1 + 2g_m R_o}$$

One sided o/p is obtained from drain of M_2

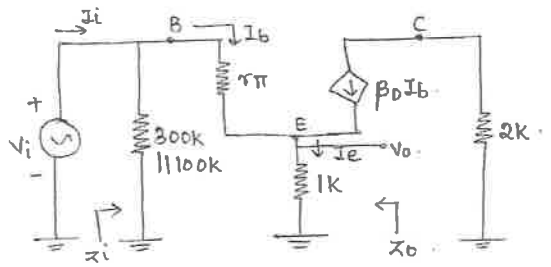
$$V_o = -g_m V_{gs_2} R_D$$

But $V_{gs_2} = V_2 - V_s$

$$\therefore V_o = -g_m R_D (V_2 - V_s)$$

05

STEP 2: AC ANALYSIS



Overall ip resistance.

Taking emitter resistance to base side

$\therefore R_E(1+\beta_D)$.

$$Z_i = R_B \| [r_\pi + (1+\beta_D)R_E]$$

$$= 300k \| 100k \left[340.358k + 120\times120\times1k\right]$$

$$= 75k \| [14.740\times10^6]$$

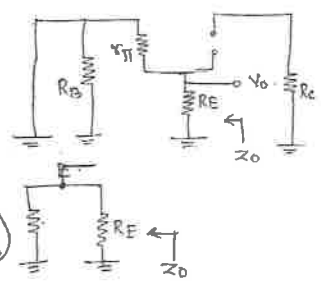
~~$Z_i = 1.405\times10^{12}\ \Omega$~~

$$\boxed{Z_i = 74.620k}$$

Overall o/p resistance.

(set $V_i = 0$.

r_π resistance from base is transferred to emitter.



$$Z_o = \left(\frac{r_\pi}{1+\beta_D}\right) \| R_E$$

$$Z_o = \frac{340.358k}{120\times120} \| 1k.$$

$$= 23.63 \| 1K$$

$$\boxed{Z_o = 23.084\Omega}$$

Q.4 a) Explain the working of two transistor (BJT) current source with the help of necessary current relationships. Also explain the effect of finite output resistance on current source performance and techniques to improve the same. [10]

06

$$A_d = \frac{g_m R_D}{2} = \sqrt{2K_n I_Q}\cdot\left(\frac{R_D}{2}\right)$$

$$= \sqrt{\frac{K_n I_Q}{2}}\cdot R_D$$

$$A_c = \frac{-\sqrt{2K_n I_Q}\cdot R_D}{1+2\sqrt{2K_n I_Q R_D}}$$

$$\therefore CMRR = \frac{1}{2}\left[1+2\sqrt{2K_n I_Q}\cdot R_D\right]$$

b) Determine overall input resistance and output resistance of the circuit as shown below in Fig. 3b. For both the transistors β=120 [10]

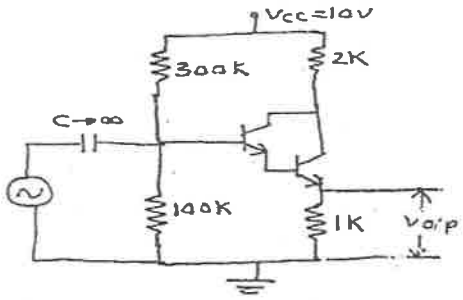


Fig. 3b

STEP 1: DC ANALYSIS

$$V_B = \frac{100K \times 10}{100K+300K}$$

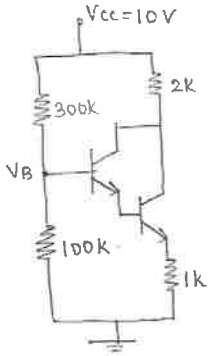
$$V_B = 2.5V$$

$$V_B - V_{BE_1} - V_{BE_2} - I_E R_E = 0$$

$$I_E = \frac{V_B - 1.4}{R_E}$$

$$= \frac{2.5-1.4}{1k}$$

$$I_E = 1.1mA$$



$$r_e = \frac{V_T}{I_E} = 23.636$$

$$r_\pi = \beta_D r_e = 120\times120\times23.636$$

$$= \sout{340.363K}$$

$$= 340.358K$$

07

→ The two transistor current source is also known as a current mirror.
→ It is the bias building block in design of IC current sources.
→ Fig below shows the ckt diagram of basic current source.
→ It consists of 2 matched (identical) transistors Q_1 and Q_2.
→ They are operated at same temp. and their bases and emitters are connected together.

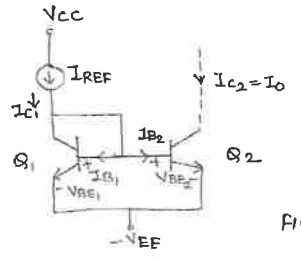


FIG-1

→ Base and collector terminals of Q_1 are connected to each other.
→ ∴ Q_1 is equivalent to a diode.
→ so as soon as supply vltg is applied, BE function of Q_1 gets forward biased and a reference current I_{REF} starts flowing.

Current relationships.

→ In fig 1, V_{BE} of both the transistors are same and transistors are identical
→ $I_{B_1}=I_{B_2}$ & $I_{C_1}=I_{C_2}$
→ KVL to collector of Q_1

$$I_{REF} = I_{C_1} + I_{B_1} + I_{B_2}$$

$$\therefore I_{REF} = I_{C_1} + 2I_{B_2}$$

$$= I_{C_1} + 2\frac{I_{C_2}}{\beta}$$

$$I_{REF} = I_{C_2}\left[1+\frac{2}{\beta}\right]$$

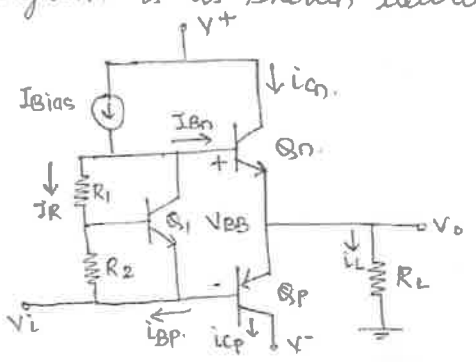
$$I_{C_2} = I_O = \frac{I_{REF}}{\left[1+\frac{2}{\beta}\right]}$$

b) Draw the circuit of V_{BE} multiplier biased class AB amplifier and explain the working and advantages of V_{BE} multiplier biased class AB amplifier. [5]

06

CLASS AB BIASING USING VBE MULTIPLIER

The ckt diagram is as shown below



c) What are the ideal characteristics of opamp and also explain the effect of high frequency on OPAMP gain and phase. [5]

CHARACTERISTICS OF IDEAL OPAMP

Characteristics of ideal opamp

i) Infinite voltage gain
ii) Infinite i/p impedance.
iii) Zero o/p impedance
iv) Infinite BW.
v) No change in the characteristic features with changes in temperature
vi) When equal voltages are applied at the 2 i/p terminals the o/p is zero
vii) Infinite slew rate.

→ The gain of the opamp rolls off after a certain frequency is reached.

→ Obviously there must be a capacitive component in the equivalent circuit of the opamp since its reactance decreases as freq increases

→ Two major sources responsible for capacitive effects:

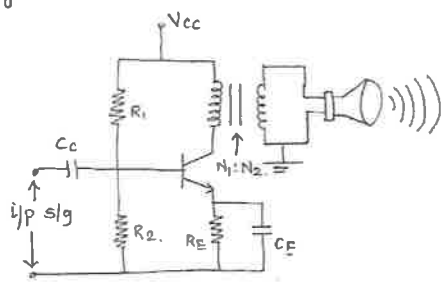
i) Physical characteristics of semiconductor device
→ Opamps are made of BJT's & FET's which contain junction capacitors
→ These junction capacitors are very small (pF range) and act as O.C at low freq.
→ But they take finite values at higher frequencies As freq increases, reactances of these capacitors decrease.

ii) Capacitive effect due to internal construction of opamp.
→ In opamps a number of transistors as well as resistors and sometimes a capacitor are integrated on the same material called the substrate.
→ In fact the substrate acts as an insulator & helps to seperate these components

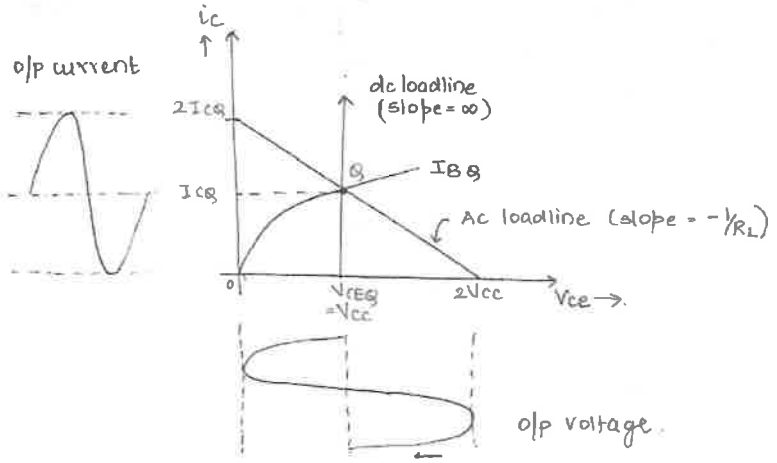
09

Q.5 a) Draw the circuit diagram of transformer coupled class A power amplifier. Also draw ac and dc loadlines for the same. Derive the expression for its power conversion efficiency. [10]

Circuit diagram



DC and AC loadline

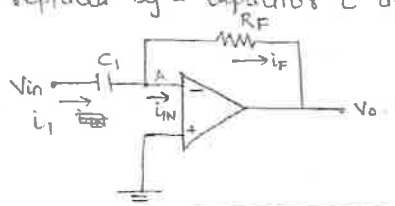


$\%.\ \eta_{max} = \frac{1}{2} = 50\ \%$

b) Explain the working of basic differentiator with the help of input and output waveforms. Also derive the expression for the output voltage. What are the limitations of basic differentiator and how to overcome these limitations. [10]

→ Differentiator as the name suggests performs the mathematical operation of differentiation i.e o/p w/f is the derivative of the i/p w/f. (rate of change of i/p vltg).

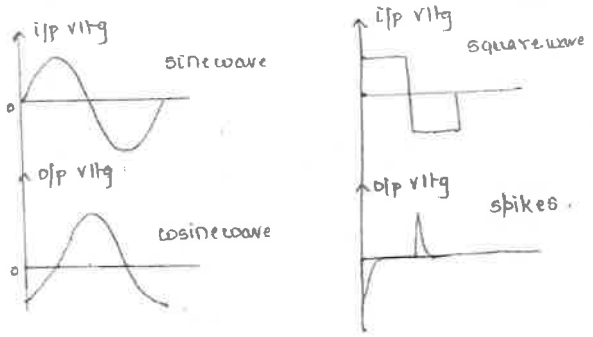
→ Differentiator ckt can be constructed from a basic inverting amplifier if the i/p resistor R_1 is replaced by a capacitor C as shown below



$$\therefore V_o = -R_F C_1 \frac{d}{dt} V_{in}$$

→ Thus the o/p vltg V_o is equal to $R_F C_1$ times the negative instantaneous rate of change of i/p vltg V_{in} with time.

Waveforms:



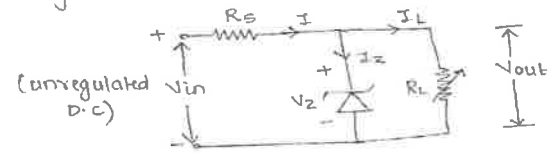
Q.6 Short notes on: (Attempt any four) [20]

a) Zener voltage regulator

→ The characteristic of zener diode i.e constant voltage at wide range of current variation through the device makes it suitable to be used as regulator (~~at~~ in the breakdown / zener region)

→ Shunt regulator is the ckt in which the regulating element is connected across the load.

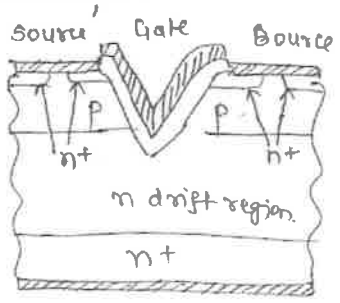
→ Fig below shows the ckt of zener shunt regulator

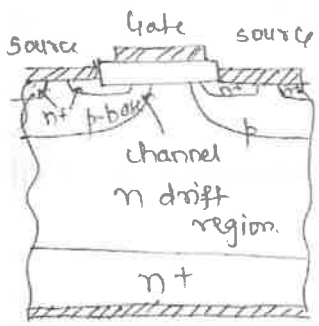


→ As long as i/p vltg Vin is greater than zener vltg Vz, the zener diode operates in breakdown region and maintains constant vltg across the load.

→ The series resistance Rs limits the i/p current.

b) Power MOSFET



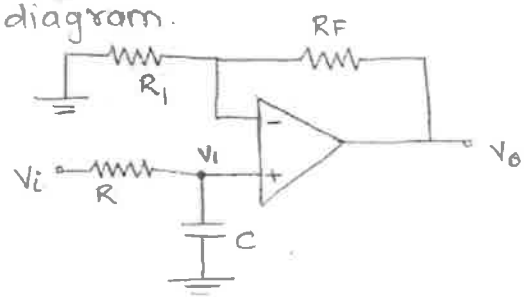


c) Class AB power amplifier

d) High pass and Low pass filter using OPAMP

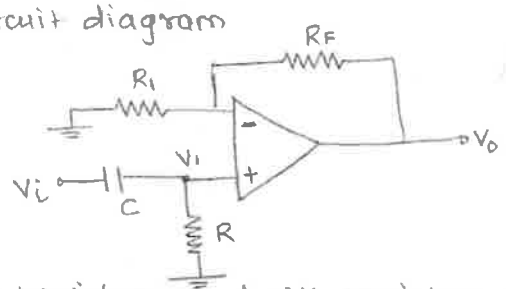
FIRST ORDER LOW PASS

→ circuit diagram.



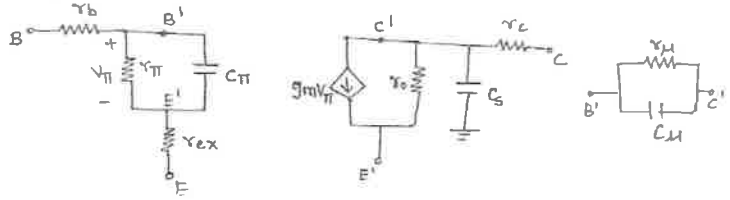
FIRST ORDER HIGH PASS

→ circuit diagram



→ i/p resistor R_1 & f/b resistor R_F are used to determine gain of filter in passband

e) High Frequency hybrid pi model of BJT



components of hybrid pi eq. a) Base - emitter b) Collector-emitter c) Base - collector