QP:23710 (1)

SE IT Sem IV CBSGS QP code: 0002371(0)
Computer Organization & Architecture.
Exam Date: 12/12/17

Marks : 80 Time : 3 Hrs.

Note : Q1 is compulsory.
Attempt any THREE out of the remaining questions.
Assume suitable data if necessary.

Q1. Attempt any 4 sub questions

a) Definition of Computer Organization : **describes the function and design of the various units of digital computer** and
Definition of Computer Architecture : **attributes visible to the programmer i.e. those attributes that have a direct impact on the logical execution of a program.**

b)

(a) Single format

(b) Double format

Figure 9.21 IEEE 754 Formats

c)

1. **Capacity**
2. **Speed**
3. **Latency**
4. **Bandwidth**

d

Instr. No.	Pipeline Stage						
1	IF	ID	EX	MEM	WB		
2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	4	5	6	7

e) data are exchanged between the processor and the I/O module.

The processor executes a program that gives it direct control of the I/O operation,.

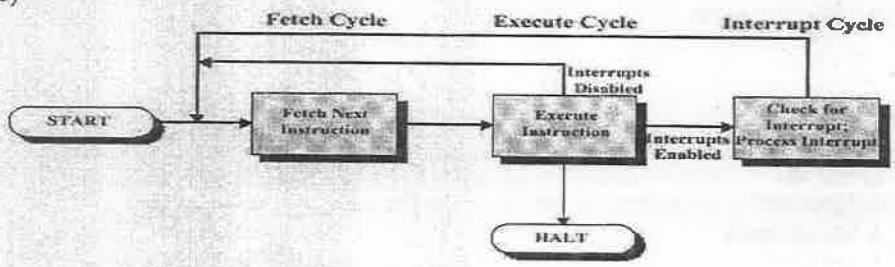
When the processor must wait until the I/O operation is complete.

It does not interrupt the processor

Q2. a)Calculate the number of page hits and faults using FIFO, LRU and OPTIMAL page replacement algorithms for the following page frame sequence : 5 , 6, 6, 3, 8, 5, 7, 8, 6, 5, 8, 5. (FRAME SIZE = 3). (10 M)

P TO

b)



Q2a.

FIFO

	5	6	6	3	8	5	7	8	6	5	8	5
	5	5	5	5	8	8	8	8	6	6	6	6
		6	6	6	6	5	5	5	5	5	8	8
				3	3	3	7	7	7	7	7	5
	F=1	F=2	H=1	F=3	F=4	F=5	F=6	H=2	F=7	H=3	F=8	F=9

PH = 03 PF = 09

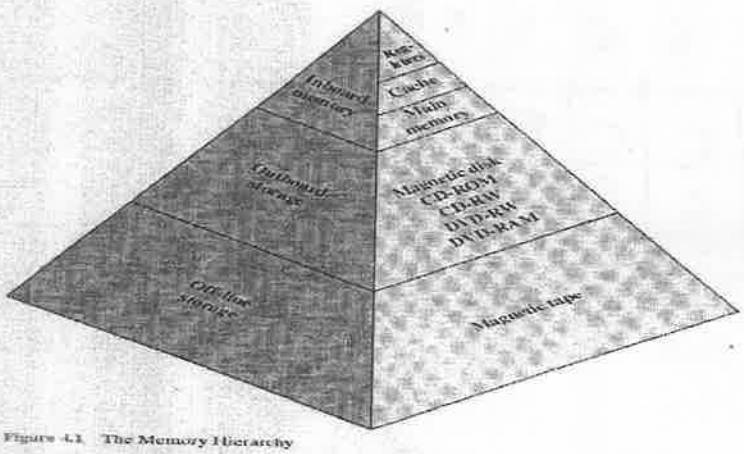
LRU

	5	6	6	3	8	5	7	8	6	5	8	5
	5	5	5	5	8	8	8	8	8	8	8	8
		6	6	6	6	5	5	5	6	6	6	6
				3	3	3	7	7	7	5	5	5
	F=1	F=2	H=1	F=3	F=4	F=5	F=6	H=2	F=7	F=8	H=3	H=4

PH = 4 PF = 08.

OPT

	5	6	6	3	8	5	7	8	6	5	8	5
	5	5	5	5	5	5	7	7	7	5	5	5
		6	6	6	6	6	6	6	6	6	6	6
				3	8	8	8	8	8	8	8	8
	F=1	F=2	H=1	F=3	F=4	H=2	F=5	H=3	H=4	F=6	H=5	H=6



Q3 a) Figure 4.1 The Memory Hierarchy

b) 1. S I S D : Single Instruction Stream Single Data Stream
2. S I M D : Single Instruction Stream Multiple Data Stream
3. M I S D : Multiple Instruction Stream Single Data Stream
4. M I M D : Multiple Instruction Stream Multiple Data Stream

Q4 a) Immediate Addressing
Direct Addressing
Register Addressing
Indirect Addressing
Register indirect addressing
Displacement Addressing
Stack Addressing

b)

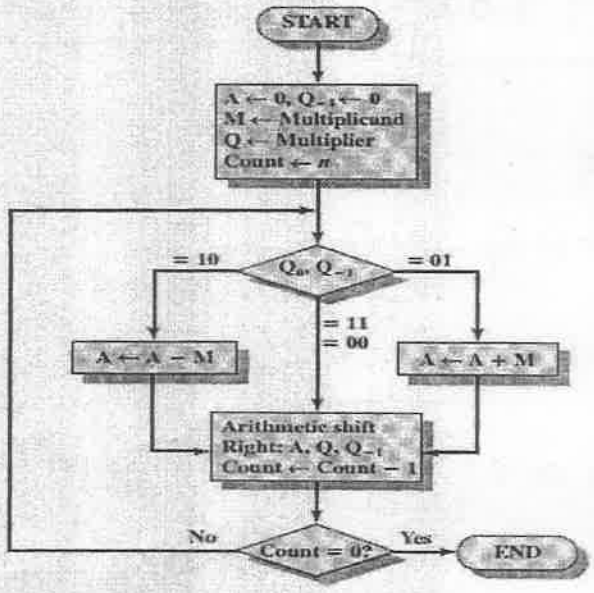


Figure 9.12 Booth's Algorithm for Twos Complement Multiplication

multiply (6)*(-4) PTO

using Booths algorithm.

Q5. a) the processor issues an I/O command,
continues to execute other instructions, and
is interrupted by the I/O module when it has completed its work.

b)

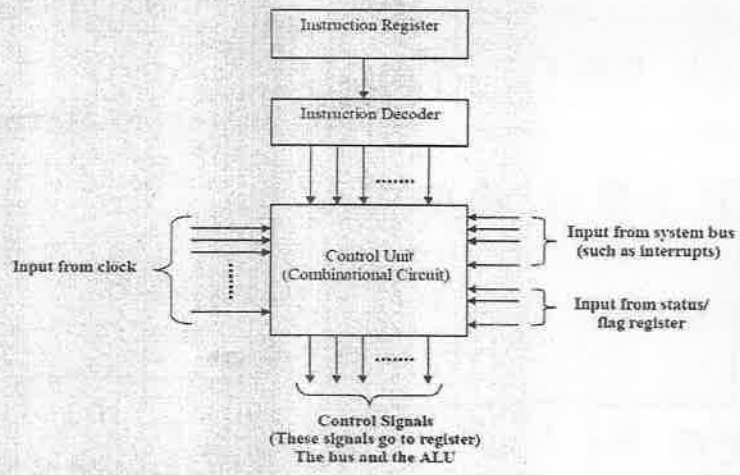


Figure (1) Hardwired Control Organization

Q4 (b) Booths algorithm (6) * (-4)

$m = 6 = 0110$. $-m = 1001$

$+1$

$4 = 0100$

$Q = -4 = 1100$ $\quad -m = 1010$.

	A	Q	Q_{-1}	
	0000	1100	0	
I1	↓			ARS A, Q, Q_{-1}
	0000	0110	0	
				ARS
I2	0000	0011	0	
				A = A - m .
				0000 .
				+1010
	1010	0011	0	1010 .
I3	↓			
	1101	0001	1	
				ARS .
I4	1110	1000	1	.

Result = 11101000

00010111

+ 1

00011000 = -24 .

—

7

7

Q6 Write notes on (any three) (20 M)

a) User-visible registers:

General purpose

Data

Address

Condition codes

Control and status registers:

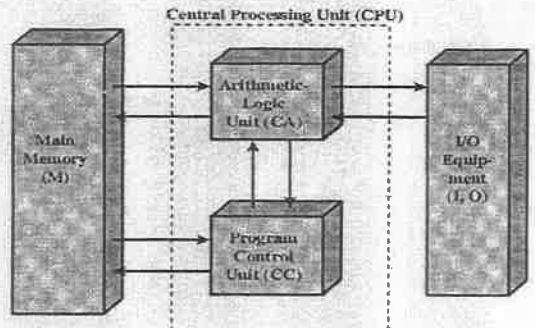
IR

PC

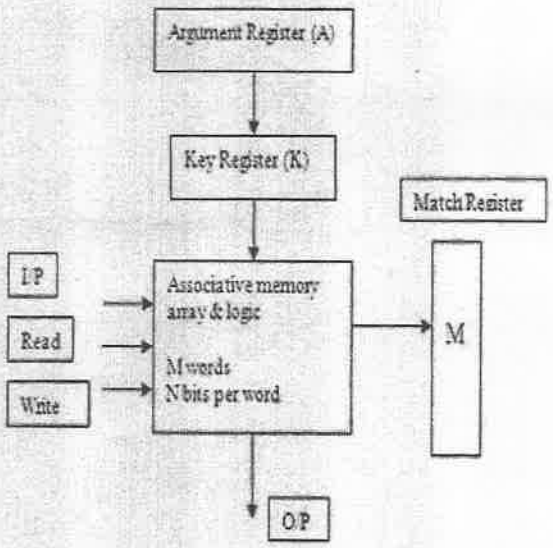
MAR

MBR

b)



c)

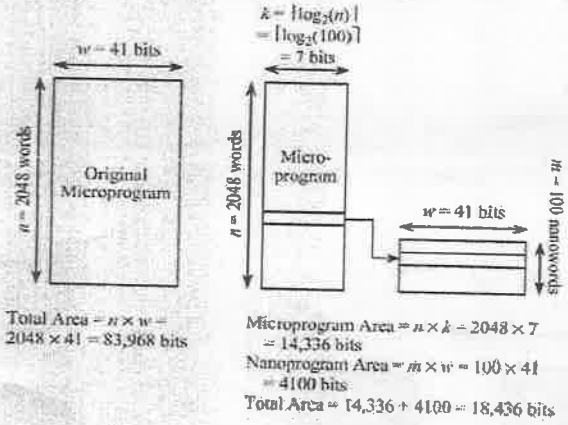


d) Nano Programming

Microprogramming vs. Nanoprogramming

(a) Micropro-gramming,

(b) nano-programming.



e) Structural hazards
Data hazards
Control hazards