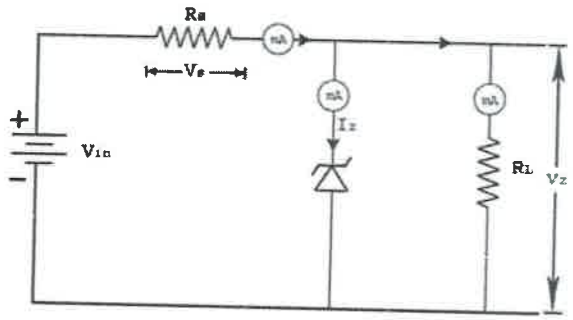
9p·Gde.- 00025073

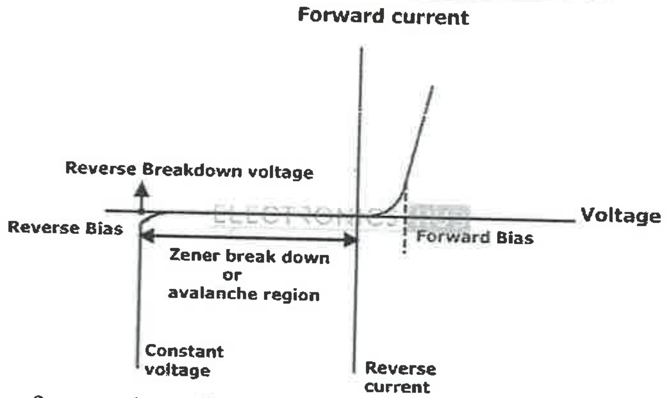
(1)

Model solution and scheme of marking

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions from the remaining five questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1		Attempt any 5 questions	
	(a)	**Types of capacitors:** Electrolytic, Ceramic, etc…. Explanation in brief.	[4]
	(b)	Explain why collector resistor R_C should be as large as possible in the design of CE amplifier.	[4]
	(c)	**Zener as voltage regulator:**	





[2]

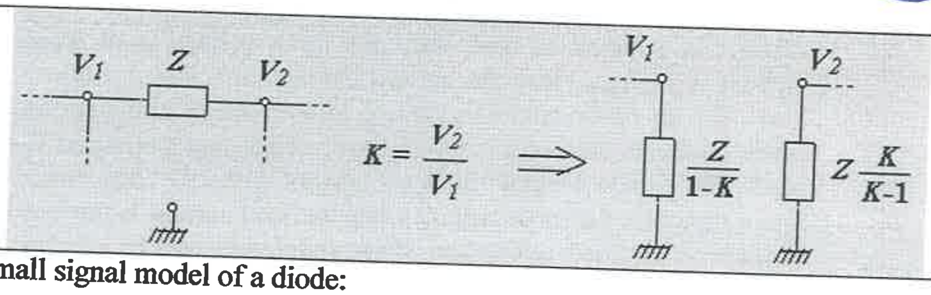
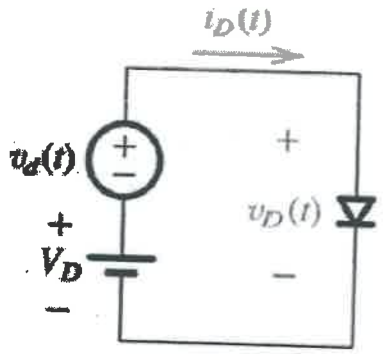
The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum $I_{Z(min)}$ value in the reverse breakdown region. It permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above a certain value - the breakdown voltage known as the Zener voltage. The Zener diode specially made to have a reverse voltage breakdown at a specific voltage. Its characteristics are otherwise very similar to common diodes. In breakdown the voltage across the Zener diode is close to constant over a wide range of currents thus making it useful as a shunt voltage regulator.

The purpose of a voltage regulator is to maintain a constant voltage across a load regardless of variations in the applied input voltage and variations in the load current. A typical Zener diode shunt regulator is shown in Figure 3. The [2]

②

OOPM PRACTICAL EXAM

		resistor is selected so that when the input voltage is at $V_{IN(min)}$ and the load current is at $I_{L(max)}$ that the current through the Zener diode is at least $I_{z(min)}$. Then for all other combinations of input voltage and load current the Zener diode conducts the excess current thus maintaining a constant voltage across the load. The Zener conducts the least current when the load current is the highest and it conducts the most current when the load current is the lowest. If there is no load resistance, shunt regulators can be used to dissipate total power through the series resistance and the Zener diode. Shunt regulators have an inherent current limiting advantage under load fault conditions because the series resistor limits excess current. A zener diode of break down voltage V_z is reverse connected to an input voltage source V_i across a load resistance R_L and a series resistor R_S. The voltage across the zener will remain steady at its break down voltage V_Z for all the values of zener current I_Z as long as the current remains in the break down region. Hence a regulated DC output voltage $V_0 = V_Z$ is obtained across RL, whenever the input voltage remains within a minimum and maximum voltage. Basically there are two type of regulations such as: **a) Line Regulation** In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value. Percentage of line regulation can be calculated by = $\frac{\Delta V_0}{\Delta V_{IN}} * 100$ where V_0 is the output voltage and V_{IN} is the input voltage and ΔV_0 is the change in output voltage for a particular change in input voltage ΔV_{IN}. **b) Load Regulation** In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value. Percentage of load regulation = $\left[\frac{V_{NL} - V_{FL}}{V_{NL}}\right] * 100$ where V_{NL} is the null load resistor voltage (ie. remove the load resistance and measure the voltage across the Zener Diode) and V_{FL} is the full load resistor voltage	
	(d)	State and explain Miller's Theorem. The Miller's theorem establishes that in a linear circuit, if there exists a branch with impedance Z, connecting two nodes with nodal voltages V_1 and V_2, we can replace this branch by two branches connecting the corresponding nodes to ground by impedances respectively $Z / (1-K)$ and $KZ / (K-1)$, where $K = V_2 / V_1$.	[2]

			[2]
	(e)	Small signal model of a diode:  Explanation.	[2] [2]
	(f)	Explain of hybrid pi model of BJT with diagram.	[2+2]
Q.2	(a)	Fabrication steps of passive elements: Fabrication Steps are: Silicon Wafer preparation, Epitaxial Growth, Oxidation, Diffusion, Ion implantation, Isolation technique, Metallization, Assembly processing and packaging. Explanation in brief.	[5]
	(b)	Explanations of concept of zero temperature drift in JFET.	[5]
	(c)	Design of an L section *LC* filter with full wave rectifier: Ripple factor $\gamma = \frac{1}{6\sqrt{2}\,\omega^2 LC}$ Critical inductance $L_c = \frac{R_L}{3\omega}$ $R_L = \frac{V_{o(dc)}}{I_L}$ Calculate value of L and using formula of ripple factor calculate value of C.	[2] [2] [2] [4]
Q.3	(a)	Small signal hybrid parameter equivalent circuit for CE amplifier Define the same. Advantages of h parameters	[3] [3] [4]

(b)

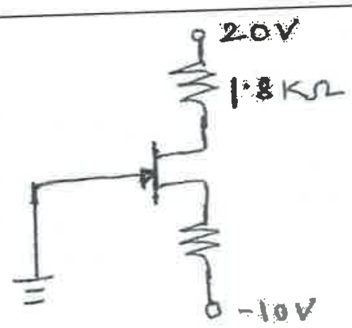


Fig. 3(b)

$V_{GS} = 10 - I_D R_S$

$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$ [4]

$I_D = 6.973\ mA$

$V_{GS} = -0.37055\ V$ [3]

$V_{DS} = V_{DD} - I_D(R_D + R_S)$ [3]

$= 7.185\ V$

Q.4 (a) Design the resistors of a single stage CS amplifier for audio frequency with BFW11 with $I_{DS} = (3.3 \pm 0.6)$ mA and $|A_V| = 12$. [03]

STEP 1: DATA FROM DATASHEET

$I_{DSS} = 7mA$, $g_{mo} = 5600\ \mu℧$, $V_P = -2.5V$, $r_d = 50k$

STEP 2: SELECTION OF BIASING TECHNIQUE

Since variation in parameter is given, we will select potential divider biasing.

STEP 3: CALCULATION FROM GRAPH OF TRANSFER CHARACTERISTICS.

(OBSERVATION TABLE FOR GRAPH TO BE TAKEN FROM DATASHEET MENTIONED AS JFET MUTUAL CHARACTERISTICS.

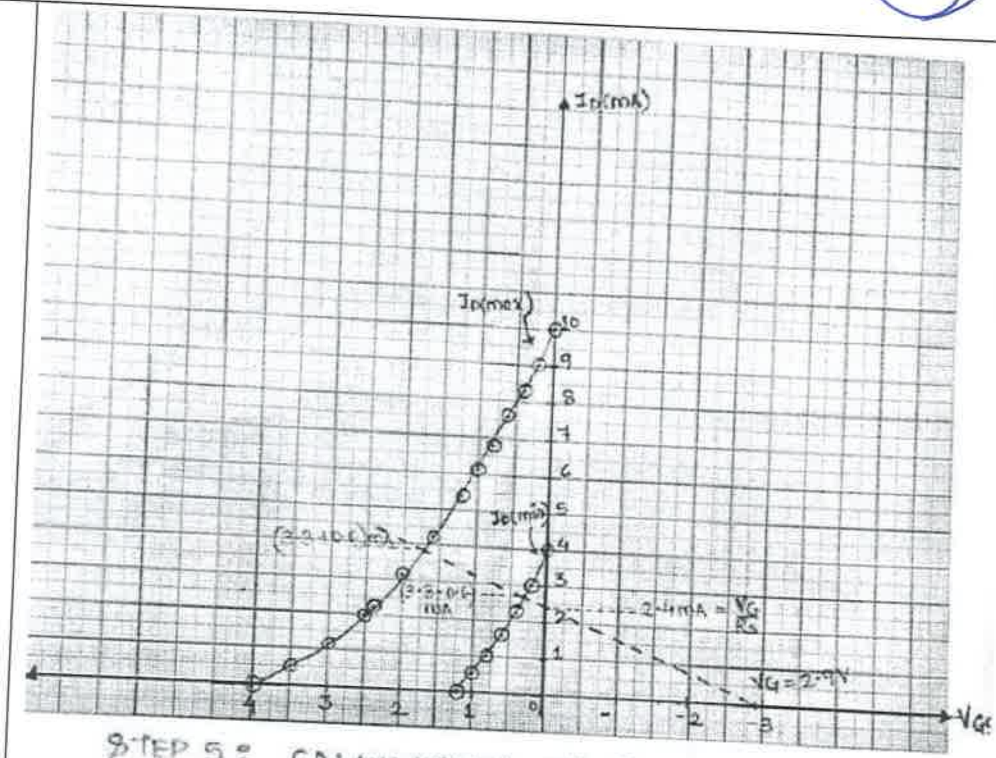
From graph $V_G = 2.9V$ and $\frac{V_G}{R_S} = 2.4mA$

$\therefore R_S = \frac{V_G}{2.4mA} = \frac{2.9}{2.4 \times 10^{-3}} = 1.208\ k\Omega$

Let $\boxed{R_S = 1.2k\Omega / \frac{1}{4}W}$

$V_{GSQ} = V_G - I_{DQ} R_S$.

$I_{DQ} = \frac{I_{D(max)} + I_{D(min)}}{2} = \frac{3.9m + 2.7m}{2} = 3.3mA$



[03]

STEP 5 : CALCULATION OF R_D.

$$|A_V| = g_m (r_d \| R_D)$$

STEP 6 : CALCULATION OF V_{DSQ}

since V_o is not given let $V_o = 2V$.

$$\therefore V_{DSQ} = 1.5 \left[V_{o(p)} + |V_P| \right]$$

STEP 7 : CALCULATION OF V_{DD}

$$V_{DD} = I_{DQ} (R_S + R_D) + V_{DSQ}$$

STEP 8 : CALCULATION OF R_1 and R_2.

$$V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2}$$

$$\frac{R_1}{R_2} = \frac{V_{DD}}{V_G} - 1.$$

[04]

(b)

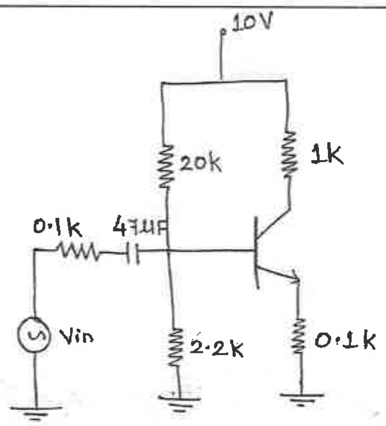


Fig. 4(b)

DC Analysis (calculate g_m and r_π) [03]

AC analysis [03]

Derivation of expression for time constant [04]

$$\tau_s = (R_s + Z_i) \cdot C_c$$

$$f_L = \frac{1}{2\pi\tau_s}$$

$$|A_{v(max)}| = \frac{g_m r_\pi R_c}{(R_s + Z_i)} \times \frac{R_B}{(R_B + Z_b)}$$

Q.5 (a) [10]

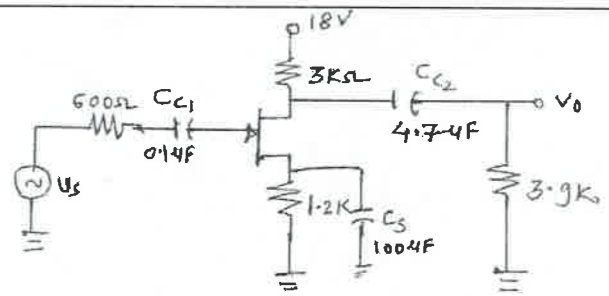


Fig. 5(a)

$$V_{GS} = -I_D R_S$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = 2.011\ mA \quad (\text{Valid Root})$$ [3]

$$V_{GS} = -2.48\ V$$ [3]

$$g_{m0} = \frac{2 I_{DSS}}{|V_P|} = 2000\ \mu\mho$$ [2]

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = 1173.6\ \mu\mho$$ [2]

(b)

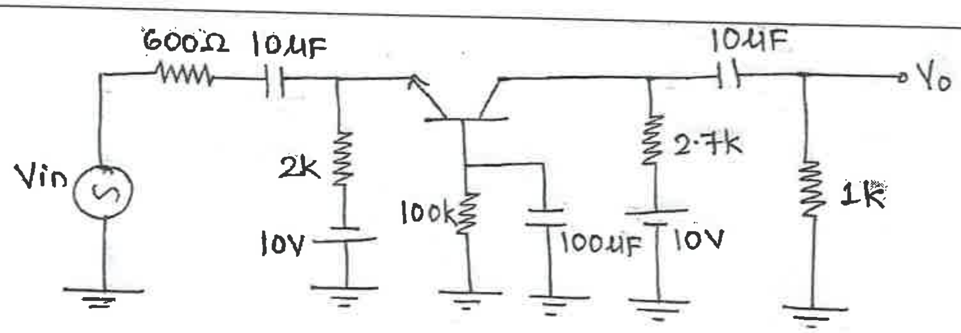
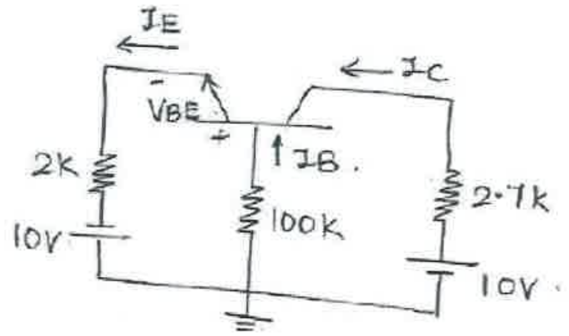


Fig. 5(b)

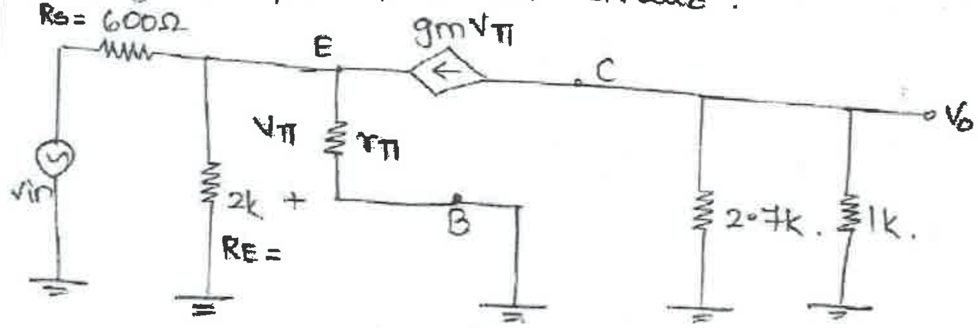
STEP 1: DC ANALYSIS.

[3]



STEP 2: AC ANALYSIS.

Hybrid pi equivalent circuit.



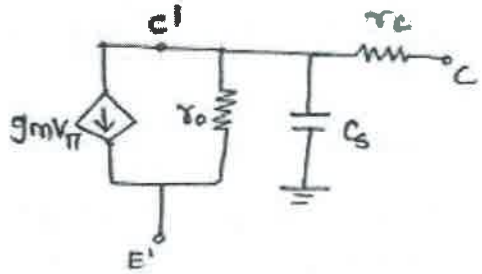
[3]

$V_o = -g_m V_\pi (2.7k \| 1k)$

$R_i = \frac{r_\pi}{1+\beta}$

$R_o = 2.7k \| 1k$

[4]

Q.6		Short notes on: (Attempt any four)	[20]
	(a)	High frequency π equivalent model of common emitter BJT. 	
	(b)	Stability factors of various biasing techniques of BJT.	
	(c)	Comparison of BJT CE and JFET CS amplifier.	
	(d)	Different types of filters.	
	(e)	JFET parameters: μ, rd, gm. Drain resistance rd = $\Delta V_{DS} / \Delta I_D$ Tran conductance gm= $\Delta I_D / \Delta V_{GS}$ Amplification factor $\mu = \Delta V_{DS} / \Delta V_{GS} = (\Delta V_{DS} / \Delta I_D) \times (\Delta I_D / \Delta V_{GS}) = rd \times gm$	