Q.P. 22626

N.B. : (1) Question No. 1 is compulsory.

(2) Solve any three questions from the remaining five

(3) Figures to the right indicate full marks

(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1	Attempt any 5 questions	[20]

a) Compare ideal and practical opamp

Characteristics of ideal opamp

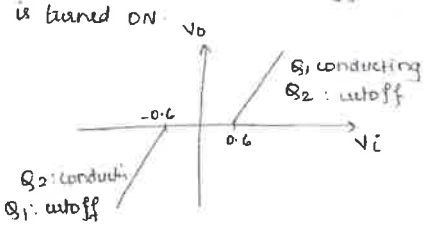
i) Infinite voltage gain
ii) infinite i/p impedance
iii) zero o/p impedance
iv) Infinite BW
v) No change in the characteristic features with changes in temperature
vi) When equal voltages are applied at the 2 i/p terminals the o/p is zero.
vii) Infinite slew rate

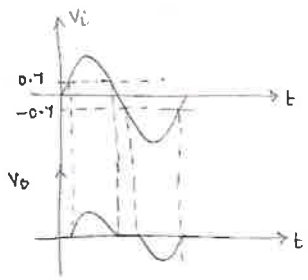
b) What is crossover distortion in power amplifier. How is it overcome?

→ In class B power amplifier base current will not flow till i/p becomes equal to cut in voltage of transistor.

→ Under this condition, sinusoidal i/p voltage will not produce sinusoidal o/p voltage.

→ o/p voltage is distorted during cross over i.e when one transistor is cutoff and other transistor is turned ON.





Remedy to overcome cross over distortion.

→ Cross over distortion can be eliminated by making some changes in existing class B ckt.

→ The change is that a small forward voltage is applied to each transistor to overcome its cut in voltage.

→ Therefore the Q pt is shifted slightly above X axis and the operation is no more a class B but class AB operation.

c) Define differential and common mode gain and differential and common mode input impedance of differential amplifiers.

→ Differential gain : It is the gain with which the differential amplifier amplifies the differential s/g Vd. (Ideally Ad shud be ∞)

→ Common mode gain : It is the gain with which a practical diff amplifier amplifies the common mode s/g. (Ideally Ac shud be 0)

Differential mode input resistance is defined as the resistances between two input base terminals when a differential mode signal is applied.

Common mode input resistance is defined as the resistances between the common input terminals of differential amplifier operating in the common mode configuration.

d) Daw the circuit diagram of widlar current source and derive the relationship between output current and reference current.

→ In all current sources, I_o is approx equal to I_{REF}.

→ For basic 2 transistor current source if $I_o = 10\mu A$ and $V_{CC} = +5V$ and $V_{EE} = -5V$, then required value of R_1 is calculated as

$$R_1 = \frac{V_{CC} - V_{BE} + V_{EE}}{I_{REF}}$$

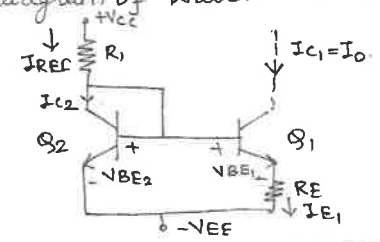
$$= \frac{5 - 0.7 + 5}{10\mu A} = 930k\Omega$$

→ A resistance of such large value is difficult to fabricate accurately on IC chip.

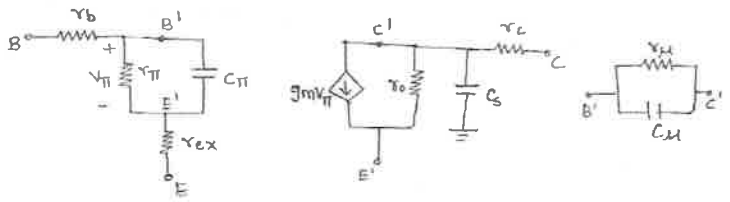
→ It requires large area as well. ∴ it is necessary to limit the value of resistor to a low kΩ range.

→ This requirement is satisfied by a special type of current source called as Widlar current source.

→ Fig. below shows ckt diagram of Widlar current source



e) Draw high frequency hybrid pi equivalent of BJT and define the various components in the model.



components of hybrid pi eq. a) Base-emitter b) Collector-emitter c) Base-collector

f) Explain line regulation and load regulation of voltage regulator. Draw the line and load regulation characteristics of ideal and practical voltage regulator.

→ The quality of IC regulator is often determined on the basis of three important parameters: line regulation, load regulation and ripple rejection

i) Line regulation : It is dependent on operating temperature of regulator.

→ Lesser line regulation implies better quality of an IC.

→ It is defined as the change in the regulated o/p vltg due to change in unregulated i/p vltg over a specific range.

ii) Load regulation : It describes change of o/p vltg over a specified load current.

→ For eg: LM7815 has load regulation of 12mV. for change of load current over a range from 5mA to 1.5A.

Q.2 a) For the circuit shown in Fig. 2a find midband gain and corner frequencies. [10]

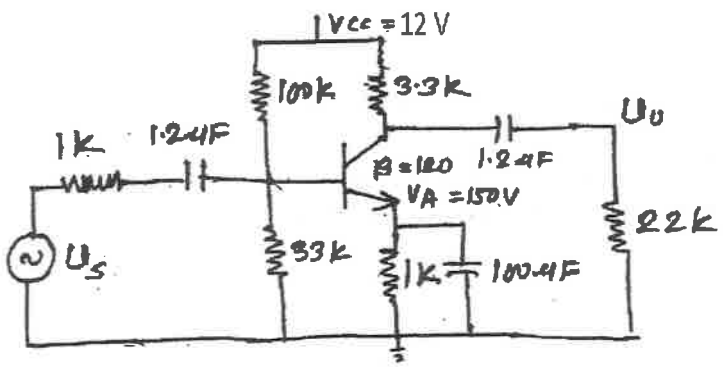


Fig.2a

b) Determine unity gain bandwidth of N channel MOSFET with parameters $K_n = 0.25$ mA/V^2, $V_{TN} = 1$V, $\lambda=0$, $C_{gd} = 0.04$ pF, $C_{gs} = 0.2$ pF, $V_{GS} = 3$V. If a 10 kΩ load is connected to the output between drain and source determine the Miller capacitance and cut-off frequency. [10]

Q.3 a) Draw circuit diagram of MOSFET based differential amplifier and derive the expression for differential gain, common mode gain and CMRR. [10]

b) For the circuit shown in Fig. 3b, find overall mid band voltage gain and [10]

capacitors C_{C1} and C_{C2} such that the 3 dB frequencies associated with each stage are equal. Assume BJT to have parameters $V_{BE\,(on)} = 0.7$ V, $\beta = 200$ and $V_A = \infty$

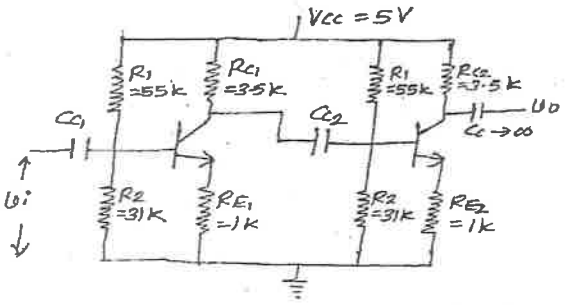


Fig. 3b

STEP 1: DC ANALYSIS

$$V_{TH} = V_{B1} = \frac{31k}{31k+55k} \times 5$$

$$V_{B1} = 1.802\,V$$

$$V_{B1} - V_{BE} - I_{E1}R_{E1} = 0$$

$$I_{E1} = \frac{V_{B1} - V_{BE}}{R_{E1}} = \frac{1.802 - 0.7}{1k}$$

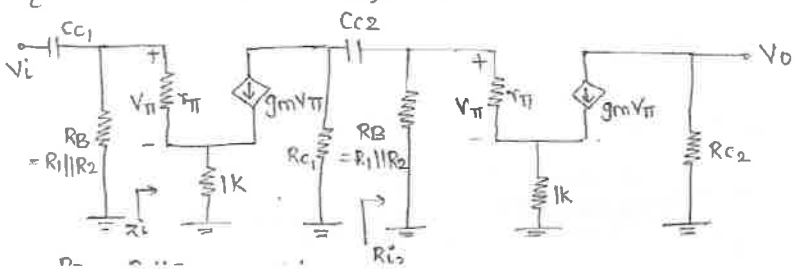
$$I_{C1} \cong I_{E1} = 1.102\,mA$$

$$I_{C2} = I_{C1} = 1.102\,mA$$

$$r_\pi = \frac{\beta V_T}{I_C} = \frac{200 \times 26mV}{1.102mA} = 4.718\,k\Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{1.102}{26mV} = 42.38\ mA/V$$

STEP 2: HYBRID PI EQUIVALENT CKT.



STEP 3: ANALYSIS OF STAGE 2:

Effective load resistance = $R_{C2} = 3.5k$.

$$V_o = -g_m V_\pi \times R_{C2}$$

$$A_{V2} = \frac{-g_m r_\pi R_{C2}}{r_\pi + (\beta+1)R_{E2}}$$

$$= \frac{42.38 \times 10^{-3} \times 4.718k \times 3.5k}{4.718k + 201 \times 1k}.$$

ANALYSIS OF STAGE 1 :

Effective load resistance on stage 1.

$$R_{L1} = R_{C1} || R_{i2} = 3.5K || R_{i2}$$

$$A_{V1} = \frac{-g_m r_\pi i_{b1} R_{L1}}{i_{b1} (r_\pi + (\beta+1) R_{E1})}$$

$$= \frac{-42.8m \times 4.718k \times 2.932K}{4.718k + 201 \times 1K}$$

$$= 2.878$$

$$A_V = A_{V1} \times A_{V2}$$

$$= 2.878 \times 3.402$$

$$= 9.790$$

STEP 4 : 3 dB frequencies associated with C_{C1} & C_{C2}

By time constant technique.

$$\tau_{S1} = C_{C1} \times (R_B || r_i)$$

$$\tau_{S1} = C_{C1} \times (R_B || (r_\pi + (\beta+1) R_E))$$

$$f_{L1} = \frac{1}{2\pi C_{C1} \times [R_B || (r_\pi + (\beta+1) R_E))} \quad \text{---- (1)}$$

By time constant technique.

$$\tau_{S2} = C_{C2} \times [R_{C1} + (R_B || (r_\pi + (\beta+1) R_E))]$$

$$f_{L2} = \frac{1}{2\pi C_{C2} \times [R_{C1} + [R_B || (r_\pi + (\beta+1) R_E))]} \quad \text{---- (2)}$$

$$f_{L1} = f_{L2}$$

$$\frac{1}{2\pi C_{C1} \times [R_B || (r_\pi + (\beta+1) R_E]} = \frac{1}{2\pi C_{C2} \times [R_{C1} + R_B || (r_\pi + (\beta+1) R_1}$$

$$C_{C1} \times 18.082K = C_{C2} (3.5K + 18.082K)$$

$$\frac{C_{C1}}{C_{C2}} = 1.193$$

Let $C_{C1} = 10\mu F$

$C_{C2} = 11.93\mu F$

Q.4	a) Draw and explain current mirror circuit using MOSFET. For the circuit shown in Fig. 4a determine the value of I_{ref} and I_O.	[10]

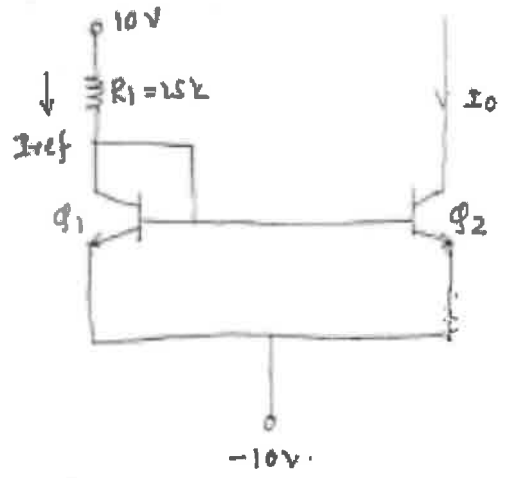


Fig.4a

b) What are the ideal characteristics of opamp and also explain the effect of high frequency on OPAMP gain and phase. [5]

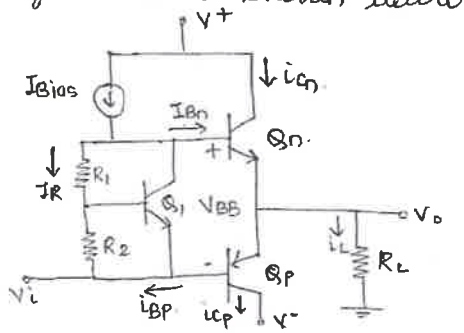
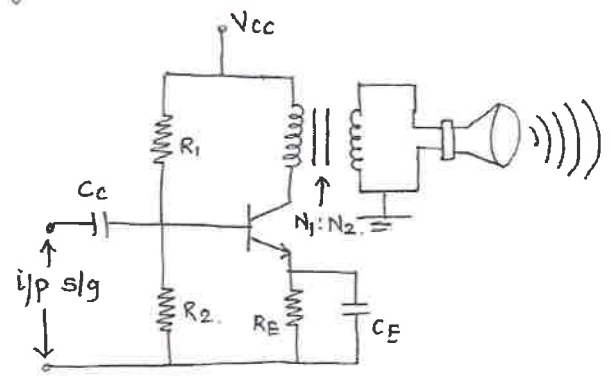
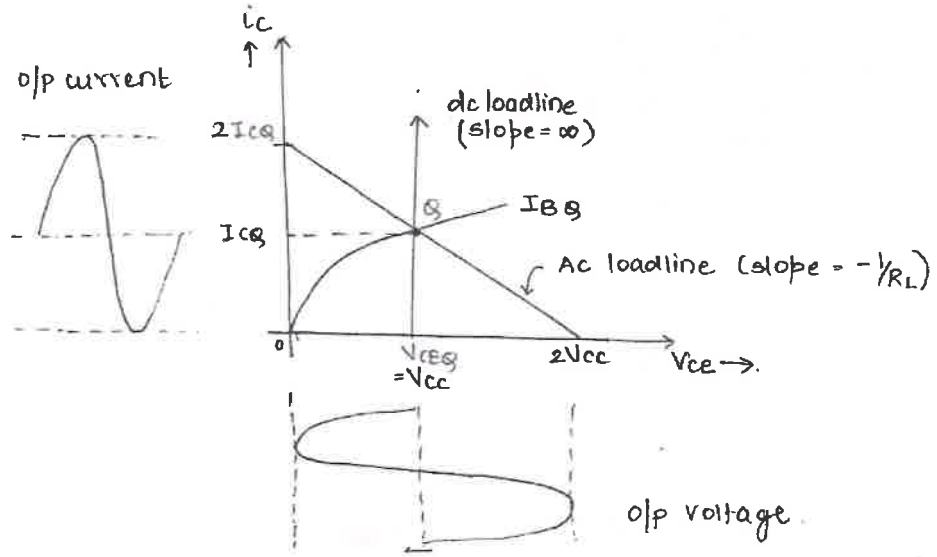
CHARACTERISTICS OF IDEAL OPAMP

Characteristics of ideal opamp

i) Infinite voltage gain
ii) Infinite i/p impedance
iii) Zero o/p impedance
iv) Infinite BW
v) No change in the characteristic features with changes in temperature
vi) When equal voltages are applied at the 2 i/p terminals the o/p is zero
vii) Infinite slew rate.

→ The gain of the opamp rolls off after a certain frequency is reached.
→ Obviously there must be a capacitive component in the equivalent circuit of the opamp since its reactance decreases as freq increases
→ Two major sources responsible for capacitive effects:
i) Physical characteristics of semiconductor devices
→ Opamps are made of BJT's & FET's which contain junction capacitors.
→ These junction capacitors are very small (pF range) and act as O.C at low freq.
→ But they take finite values at higher frequencies As freq increases, reactances of these capacitors decrease
ii) Capacitive effect due to internal construction of opamp.
→ In opamps a number of transistors as well as resistors and sometimes a capacitor are integrated on the same material called the substrate.
→ In fact the substrate acts as an insulator & helps to seperate these components

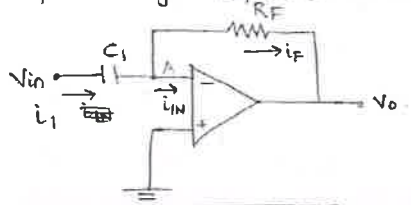
c) Draw the circuit of V_{BE} multiplier biased class AB amplifier and explain [5]

	the working and advantages of V_{BE} multiplier biased class AB amplifier. CLASS AB BIASING USING V_{BE} MULTIPLIER The ckt diagram is as shown below 	
Q.5	a) Draw the circuit diagram of transformer coupled class A power amplifier. Also draw ac and dc loadlines for the same. Derive the expression for its power conversion efficiency. Circuit diagram  DC and AC Loadline  $\% \eta_{max} = \frac{1}{2} = 50\ \%$	[10]
	b) Explain the working of basic differentiator with the help of input and output waveforms. Also derive the expression for the output voltage. What are the	[10]

limitations of basic differentiator and how to overcome these limitations.

→ Differentiator as the name suggests performs the mathematical operation of differentiation ie o/p w/f is the derivative of the i/p w/f. (rate of change of i/p vltg).

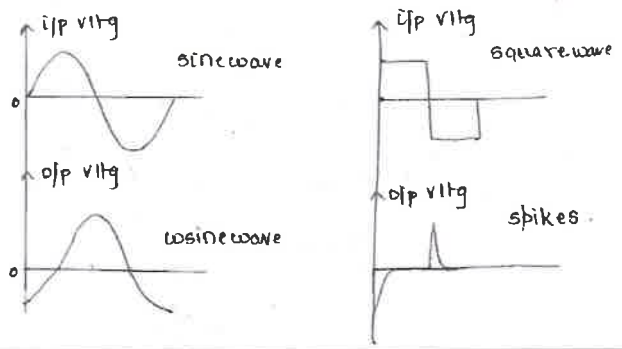
→ Differentiator ckt can be constructed from a basic inverting amplifier if the i/p resistor R_1 is replaced by a capacitor C as shown below



$$\therefore V_o = -R_F C_1 \frac{d}{dt} V_{in}$$

→ Thus the o/p vltg V_o is equal to $R_F C_1$ times the negative instantaneous rate of change of i/p vltg Vin with time.

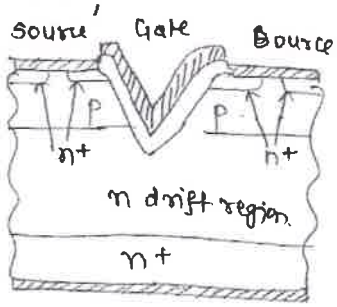
Waveforms.

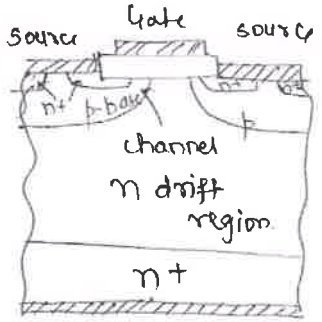


Q.6	Short notes on: (Attempt any four)	[20]

a) Transistorised series regulator

b) Power MOSFET



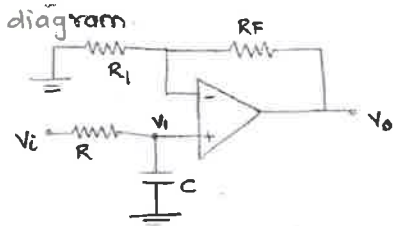


c) Class AB power amplifier

d) Active filters

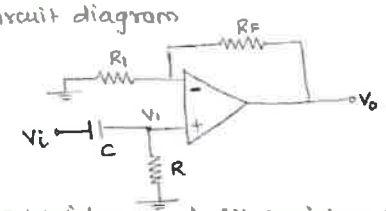
FIRST ORDER LOW PASS

→ circuit diagram



FIRST ORDER HIGH PASS

→ circuit diagram



→ i/p resistor R_1 & f/b resistor R_F are used to determine gain of filter in passband

e) Multistage amplifiers

MULTISTAGE AMPLIFIERS

→ For many amplification purposes, a single transistor does not provide enough gain, so multiple ckts or stages of amplification are needed.

→ When an amplifier contains multiple stages the total gain is product of individual stage gains

$$G = G_1 \times G_2 \times G_3 \times \cdots$$

→ In dB $G(dB) = G_1(dB) + G_2(dB) + G_3(dB) + \cdots$

TYPES OF 2 STAGE CASCADED AMPLIFIERS.

1. CE-CE cascade
2. CE - CC cascade
3. CC - CE cascade
4. CC - CC cascade (Darlington).
5. CE - CB cascade (Cascode).
6. CB - CC cascade
7. CC - CB cascade (emitter coupled pair)

Explain any one of the above.