LC Solution

Q1 a) I $\overline{AB} = \overline{A} + \overline{B}$
II $\overline{A+B} = \overline{A} \cdot \overline{B}$
De Morgan's theorem. 5 mks.

A	B	AB	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$	$\overline{A+B}$	$\overline{A}\cdot\overline{B}$
0	0	0	1	1	1	1	1	1
0	1	0	1	1	0	1	0	0
1	0	0	1	0	1	1	0	0
1	1	1	0	0	0	0	0	0

I proved II proved

Q1 b) Reflective Codes: eg. EXCESS-3 code 2 mks.
Explanation with truth table 3 mks.

Q1. c) Hazards in combinational circuits 5 mks.
- static 1 hazard
- static 0 hazard
- dynamic hazard

explanation

Q1 d) Level triggered FlipFlops:
- diagram 1 mk
- explanation 1.5 mks

Edge triggered FlipFlops
- diagram 1 mk
- explanation 1.5 mks.

Q1e) CMOS & TTL logic families: 5 mks
- Comparison (at least 5 points)

Q2 a) Two bit Multiplier (A_1A_0) with (B_1B_0) (2)

Product : $P_3P_2P_1P_0$

- Truth table (2) mks
- Kmaps (2) mks
- Equations for $P_3.P_2\,P_1\,P_0$ (4) mks
- Circuit diagram (2) mks

$P_3 = A_1A_0B_1B_0$

$P_2 = A_1\overline{A_0}B_1 + A_1B_1\overline{B_0}$

$P_1 = A_1\overline{B_1}B_0 + A_1\overline{A_0}B_0 + \overline{A_1}A_0B_1 + A_0B_1\overline{B_0}$

$P_0 = A_0B_0$

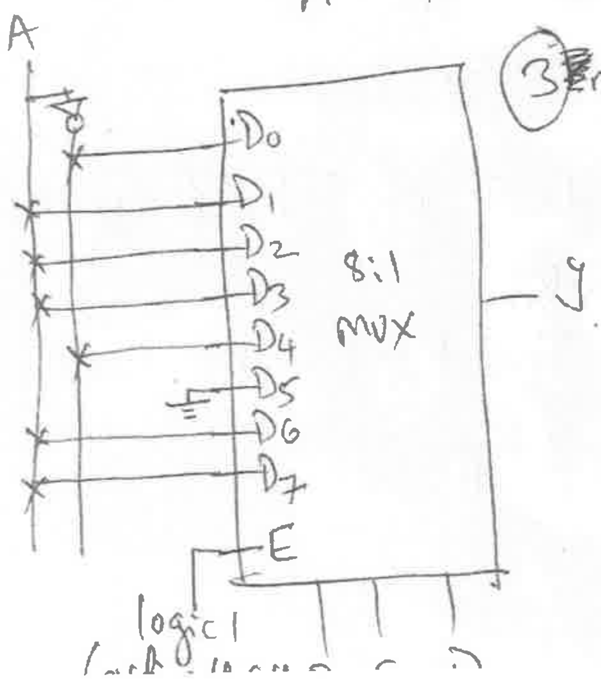
Q2 b) $y = f(A,B,C,D) = \pi M(1,2,3,5,6,7,8,12,13)$

$= \sum m(0,4,9,10,11,14,15)$

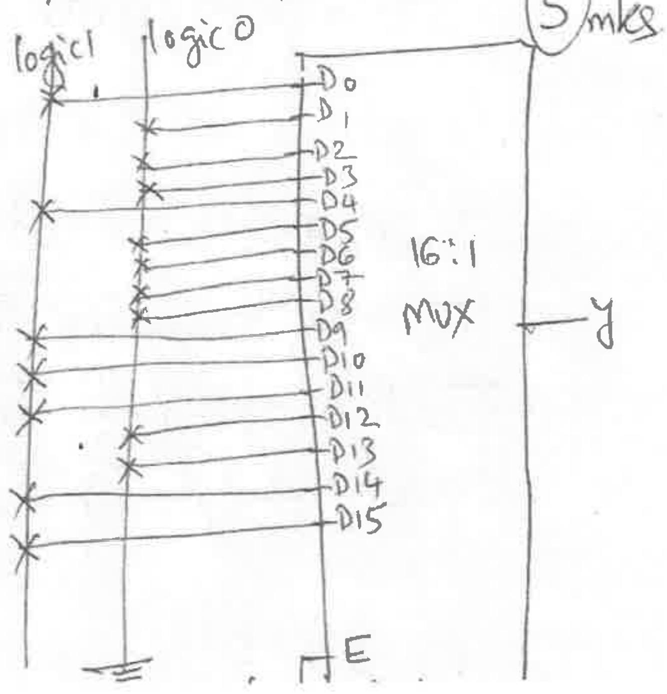
(2) mks

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	$\overline{A}$	A	A	A	$\overline{A}$	0	A	A

(5) mks



(3) mks



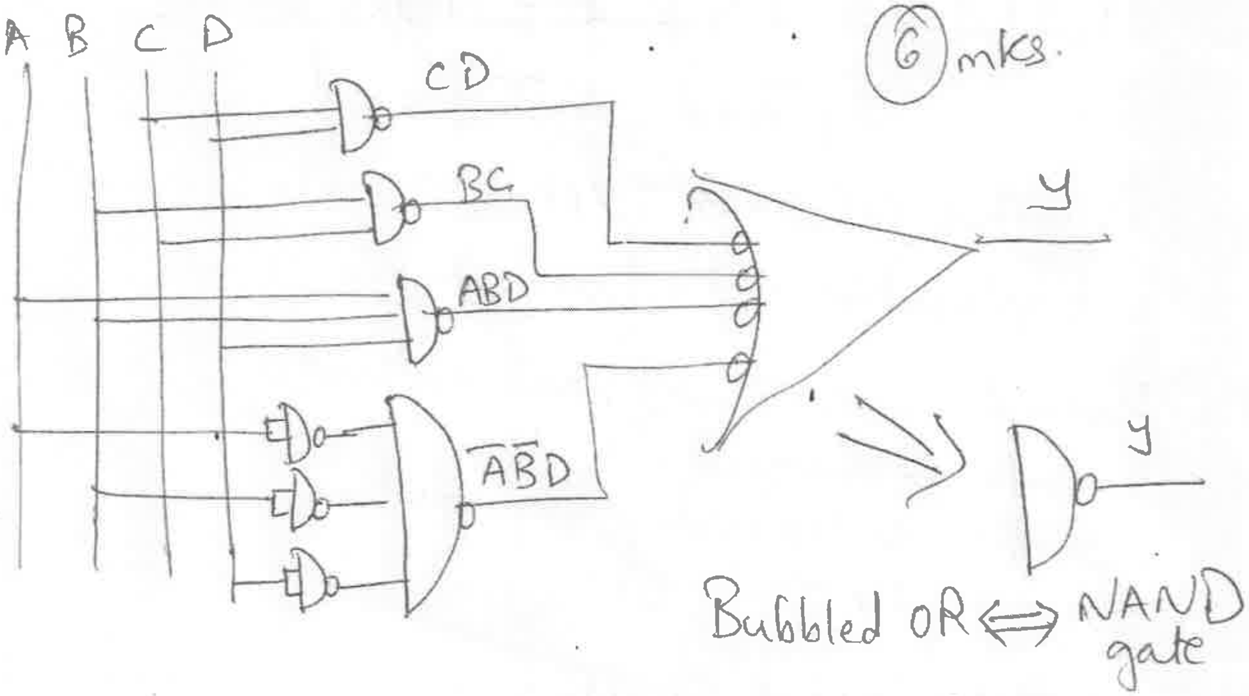
Q3-a) $y = f(A,B,C,D) = \prod M(0,2,4,5,8,9,10,12)$ (3)

$y = CD + BC + \overline{A}\,\overline{B}D + ABD$ - (4) mks.

CD \ AB	00	01	11	10
00	0	0	0	0
01	1	0	1	0
11	1	1	1	1
10	0	1	1	0

$\overline{A}\,\overline{B}D$; ABD ; CD ; BC

(6) mks.



Q3 b) Gray ($G_3G_2G_1G_0$) to Binary ($B_3B_2B_1B_0$) Converter

- Truth table - (2) mks.
- K maps (2) mks
- Equations for B_3, B_2, B_1 & B_0 - (4) mks
- Circuit diagram - (2) mks

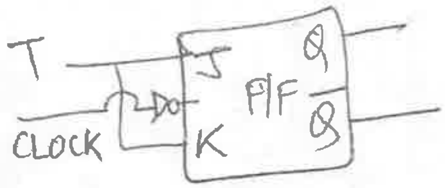
$B_3 = G_3$, $B_2 = G_3 \oplus G_2$, $B_1 = G_3 \oplus G_2 \oplus G_1$

$B_0 = G_3 \oplus G_2 \oplus G_1 \oplus G_0$

Q4 a) S-R FlipFlop
- diagram using NAND gates 1 mk
- explanation 3 mks
- truth table 1 mk
- characteristic equation 1 mk
- excitation table 1 mk
- state transition diagram 1 mk
- Race around condition explanation 2 mks

Q4 b) Bidirectional Shift Register
- diagram 2 mks
- explanation 3 mks.

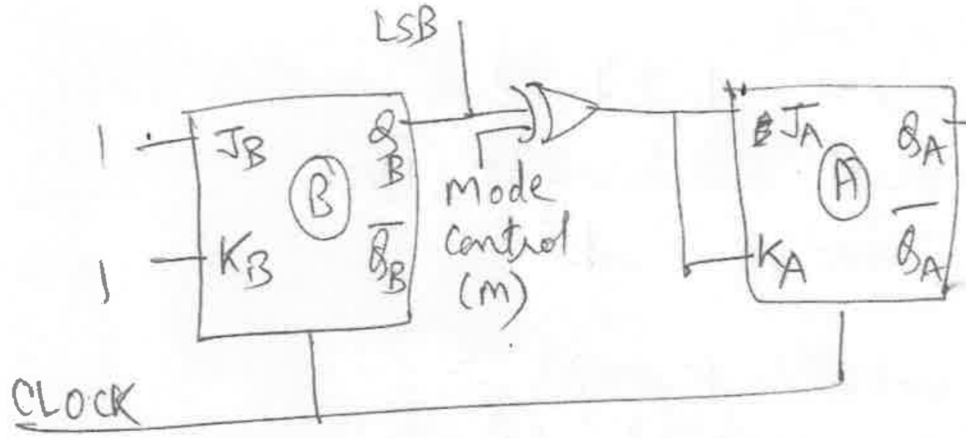
Q4 c) JK FlipFlop to T FlipFlop
- conversion logic table 2 mks.
- K map 1 mk
- Equation 1 mk
- diagram 1 mk



Q5. a) - Sequence of the counter when M=0 or M=1 1 mk
- Truth table & excitation table of JK F/F 1 mk
- Table of sequence 2 mks
- K-maps for J_A, K_A, J_B & K_B 3 mks
- equations for J_A, K_A, J_B & K_B 2 mks.

$J_B = K_B = 1$

$J_A = K_A = M \oplus Q_B$



1 mk.

Q5 b) Full Subtractor Circuit
- Truth table (i/p's ⇒ A, B, C, o/p's ⇒ D & B_0) 1 mk
- Kmaps for D & B_0 1 mk
- Equations for D & B_0 2 mks
- circuit diagram 1 mk

$D = A \oplus B \oplus C$, $B_0 = \overline{A}(B+C) + BC$

Q5 c) Master-Slave F/F: -
- diagram - 2 mks.
- explanation 3 mks

Q6 a) Steps in Quine McClusky's method -
- take an example 1/2 mk
- Solve it 3 mks
- describe the steps while solving 1 1/2 mks

Q6 b) Counter ICs -
- example 1 mk
- circuit diagram 2 mks
- explanation 2 mks

Q6 c) Hamming Code : (6)

- rules to calculate Hamming Code bits (2) mks
- example & solving it (1) mk
- explanation. (2) mks

Q6 d) 5 & 6 variable K-maps

- take 1 example (1) mk
- Solve it using 5/6 variable k maps (2) mks
- explanation (2) mks

Q6 e) Design of 3bit odd parity generator

A	B	C	y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

y

C \ AB	00	01	11	10
0	1_0	0_2	1_6	0_4
1	0_1	1_3	0_7	1_5

$$y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + AB\bar{C} + A\bar{B}C$$

$$= A(B \oplus C) + \bar{A}(\overline{B \oplus C})$$

$$= \overline{A \oplus B \oplus C}$$

$$= A \odot B \odot C$$