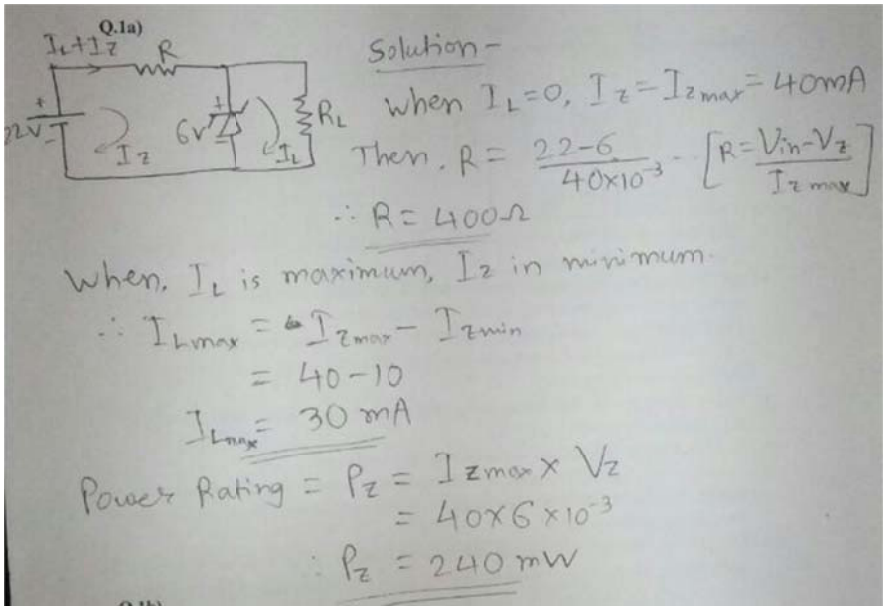
SE/SEM III/CBCGS/IN/AE/May 2018 (KT)

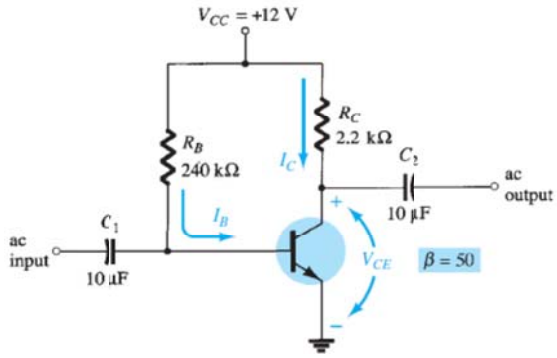
(R 2016)

Paper solution

Q.1a)



Q.1b)



$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

$$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\text{ mA}}$$

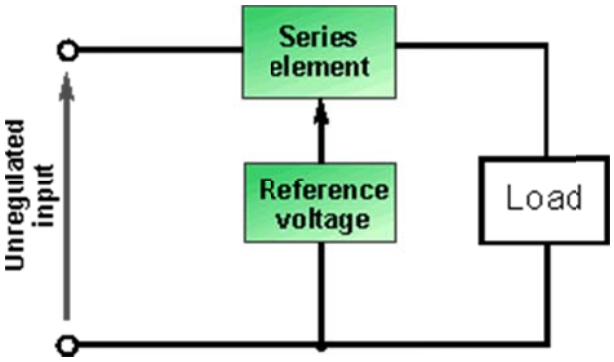
$$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\text{ V}}$$

$V_B = V_{BE} = \mathbf{0.7\text{ V}}$ $V_C = V_{CE} = \mathbf{6.83\text{ V}}$

$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$
$= \mathbf{-6.13\text{ V}}$

Q.1c) The term *field effect* is analogous to effect of magnet on its surroundings. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual contact. The magnetic field of the permanent magnet envelopes the filings and attract them to the magnet along the shortest path provided by the magnetic flux lines. For the FET an *electric field* is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

Q.1d)

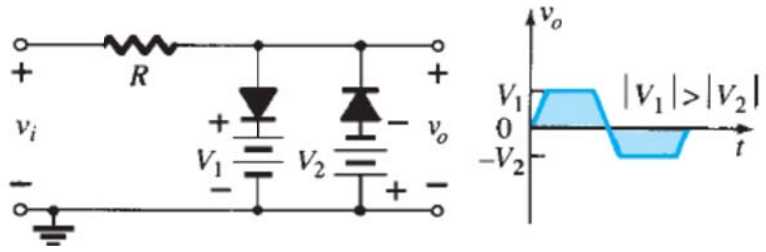


- The series voltage regulator or series pass voltage regulator uses a variable element placed in series with the load.
- By changing the resistance of the series element, the voltage dropped across it can be varied to ensure that the voltage across the load remains constant
- The advantage of the series voltage regulator is that the amount of current drawn is effectively that used by the load, although some will be consumed by any circuitry associated with the regulator.
- Unlike the shunt regulator, the series regulator does not draw the full current even when the load does not require any current.
- As a result the series regulator is considerably more efficient.
- One of the simplest implementations of this concept is to use a single pass transistor in the form of an emitter follower configuration, and a single Zener diode drive by a resistor from the unregulated supply.
- This provides a simple form of feedback system to ensure the Zener voltage is maintained at the output, albeit with a voltage reduction equal to the base emitter junction voltage - 0.6 volts for a silicon transistor.

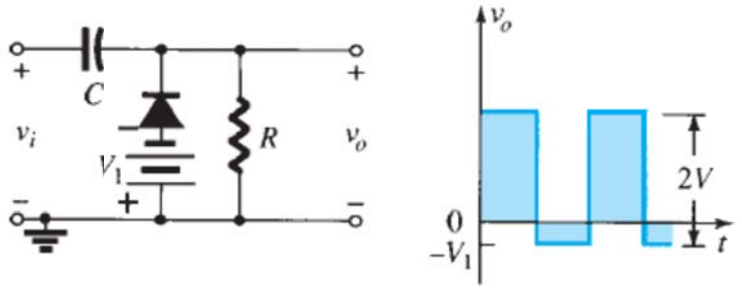
Q.1 e) Filters are classified as Active and Passive filters.

They are also classified as LPF, HPF, BPF, BRF

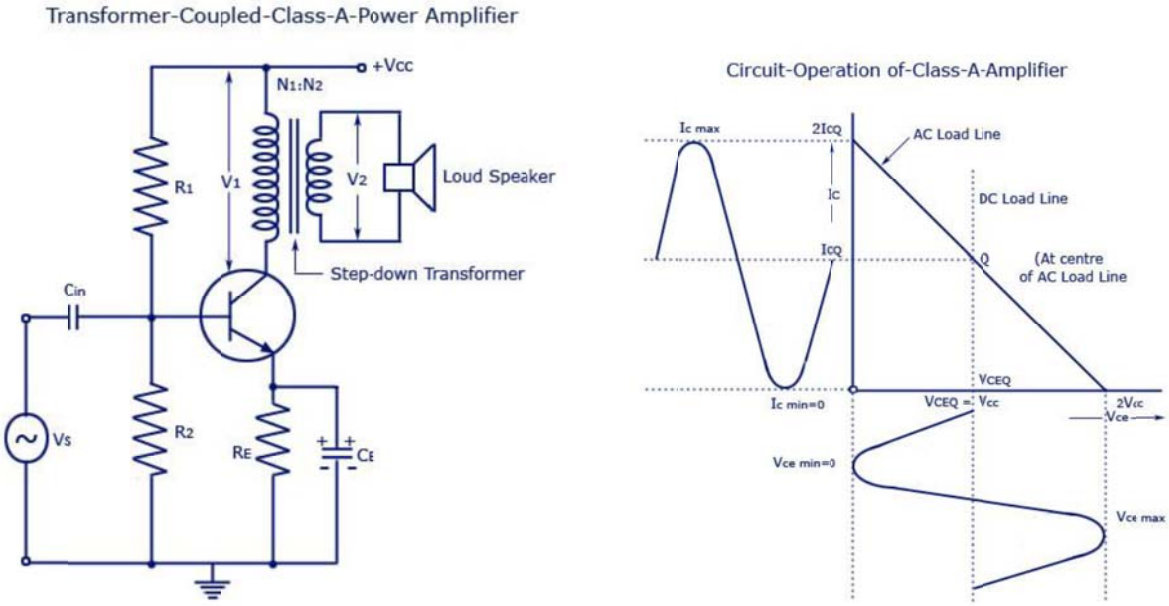
Q.2 a)



Q.2 b)

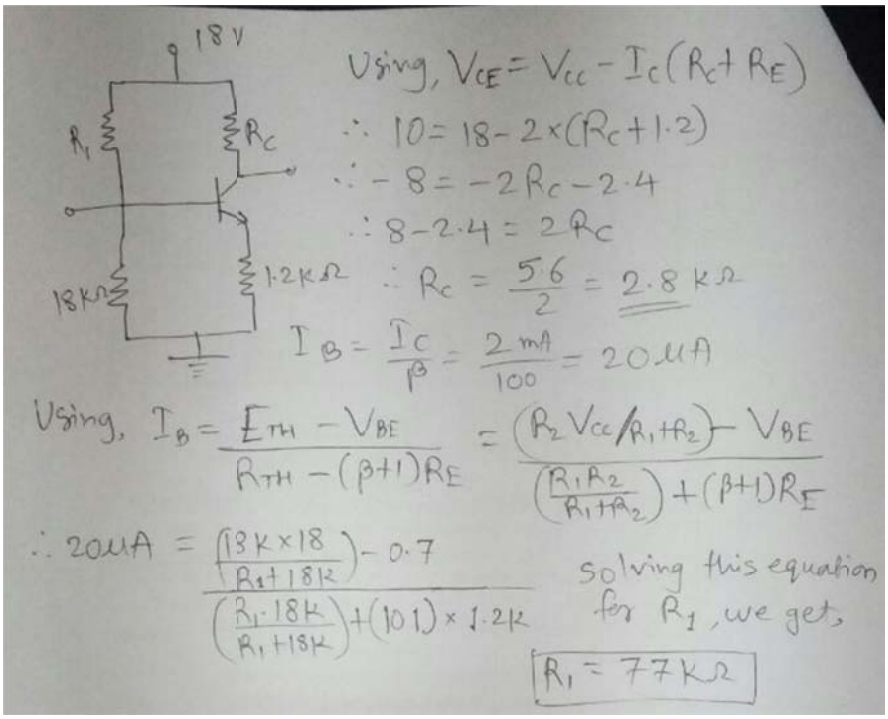


Q.2 c)



- In this circuit dc (winding) resistance determines the dc load line.
- Typically, this resistance is quite small (assumed to be zero) providing dc load to be a vertical line rising from Vcc, as shown.
- When an ac signal is applied to the base of the transistor the collector current will vary around the operating point Q.
- In order to have maximum ac power output, the peak value of collector current due to input ac signal alone should be equal to the zero-signal collector current.
- To achieve this, the operating point Q is located at the centre of the ac load line.
- This is achieved by adjusting the biasing circuit (R1, R2 and RE). When ac signal is applied, collector current fluctuates from maximum to minimum (zero), and operating point Q moves up and down the load line.
- At the peak of the positive half cycle of the input signal, the total collector current Ic max = 2 Ic and collector-emitter – voltage Vcg min = 0 while at the peak of the negative half cycle of the input signal, the collector current Ic min = 0 and collector-emitter voltage Vce max = 2 Vcc.
- Thus collector-emitter voltage varies in opposite phase to the collector current.
- The variation of collector voltage appears across primary of the transformer.
- Now ac voltage is induced in the transformer secondary which in turn develops ac power and supplies to the load.

Q.3 a)



Q.3 b)
Thermal Runaway

Q.3 c)

- Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in figure next page.
- When V_i = 5 V, the transistor will be "on" and the design must ensure that the network is heavily saturated by a level of I_B greater than that associated with the I_B curve appearing near the saturation level.
- In next Figure, this requires that $I_B > 50\ \mu A$. The saturation level for the collector current for the circuit is defined by,

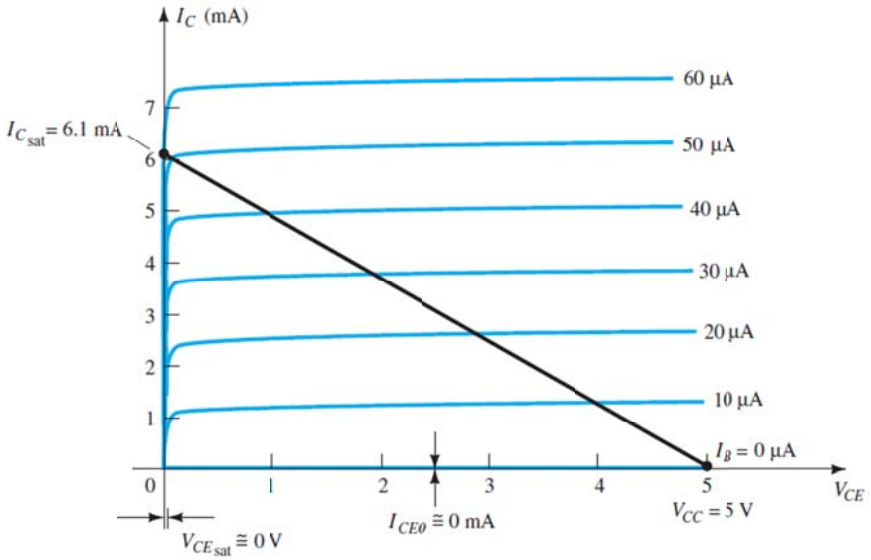
$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

- The level of *I B* in the active region just before saturation results can be approximated by the following equation.

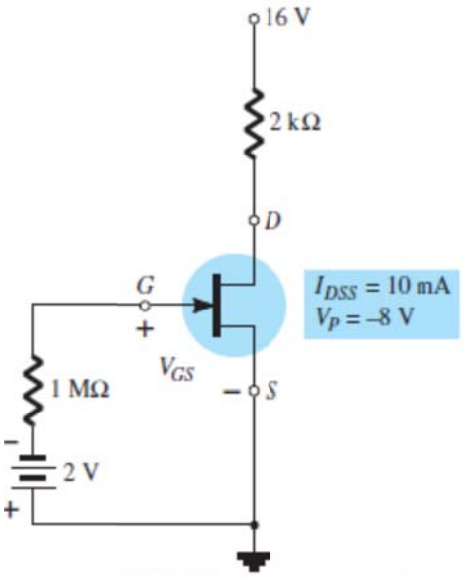
$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

  - For the saturation level we must therefore ensure that the following condition is satisfied:

$$I_B > \frac{I_{C_{sat}}}{\beta_{dc}}$$



Q.4 a)



Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $I_{D_Q} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \dfrac{-2\text{ V}}{-8\text{ V}}\right)^2$
$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$
$= \mathbf{5.625\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without

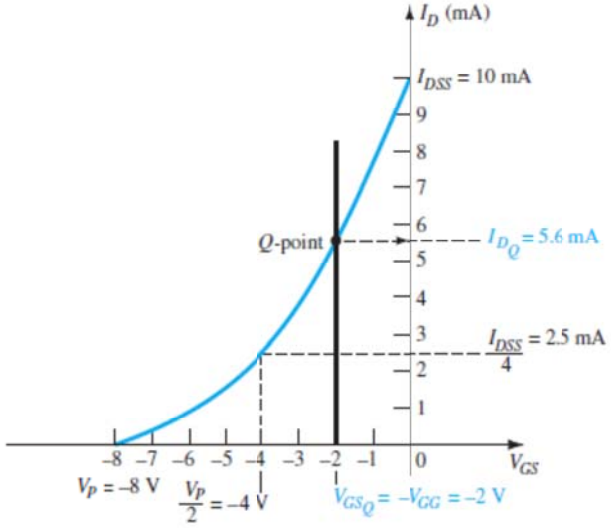


FIG. 7.7

significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7.7 is quite acceptable.

a. Therefore,

$$V_{GS_Q} = -V_{GG} = -2\text{ V}$$

b. $I_{D_Q} = 5.6\text{ mA}$

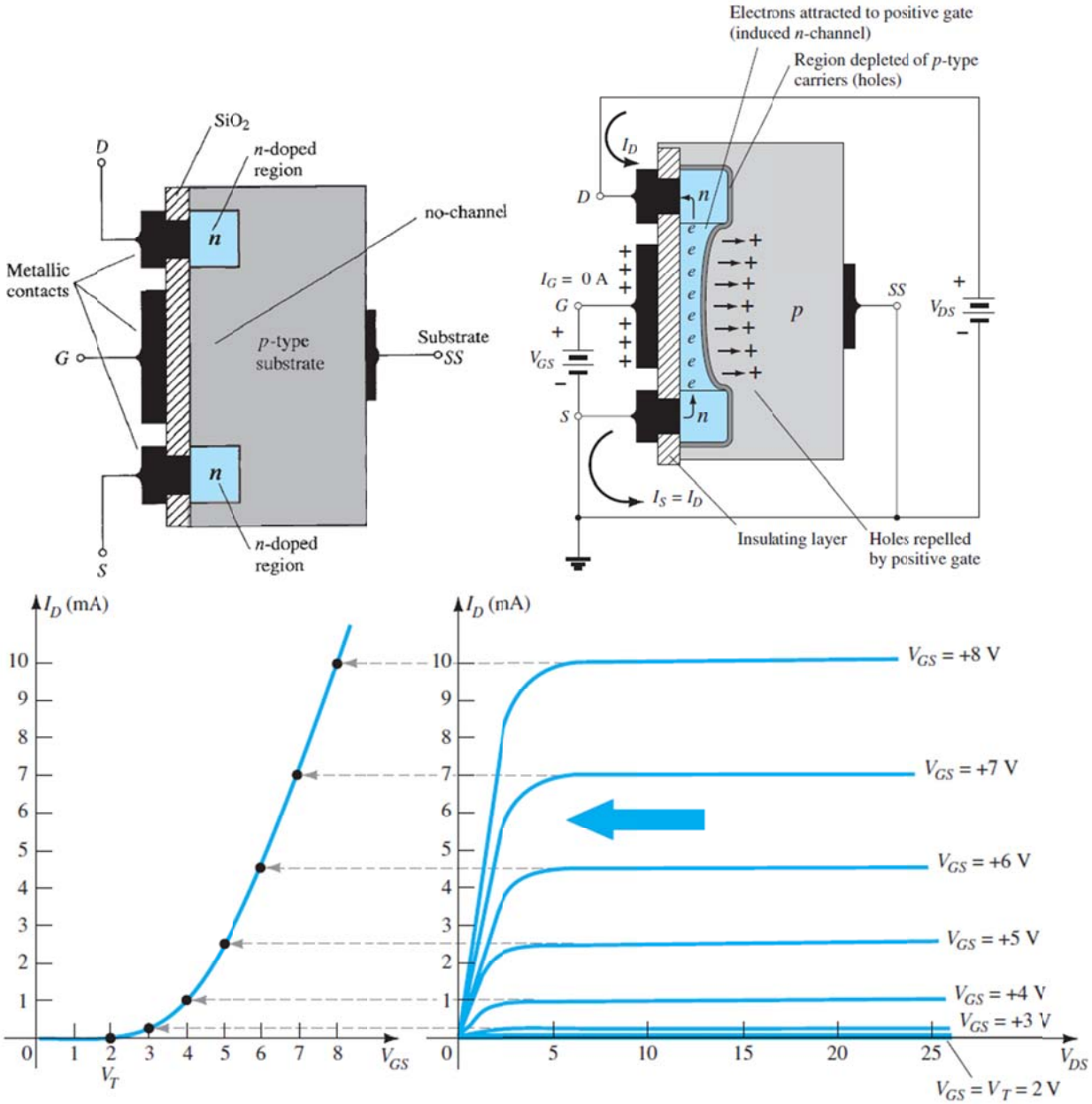
c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.6\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.2\text{ V} = 4.8\text{ V}$

d. $V_D = V_{DS} = 4.8\text{ V}$

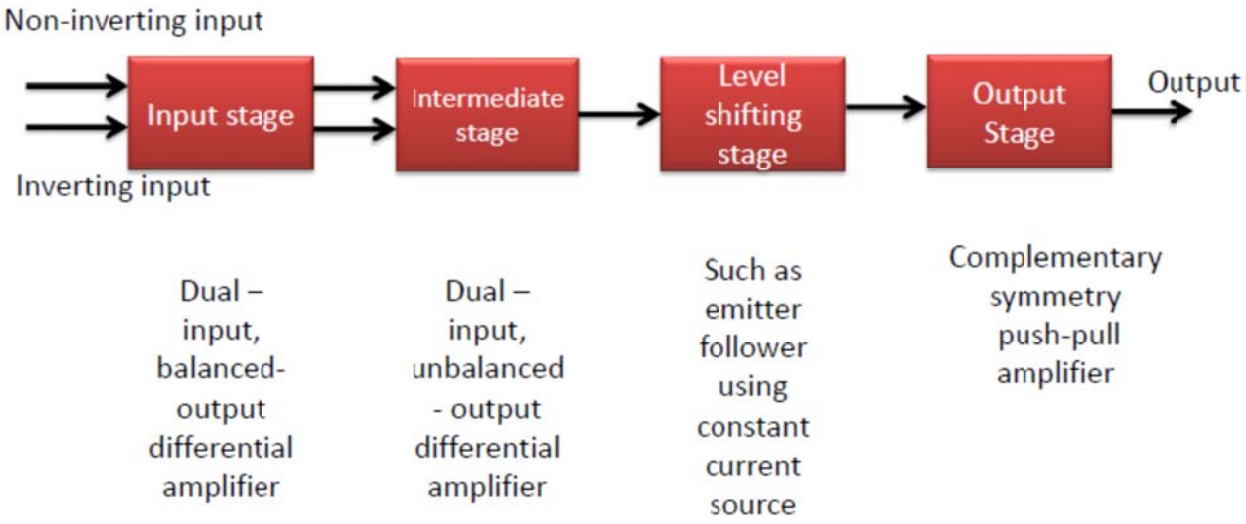
e. $V_G = V_{GS} = -2\text{ V}$

f. $V_S = 0\text{ V}$

Q.4 b)

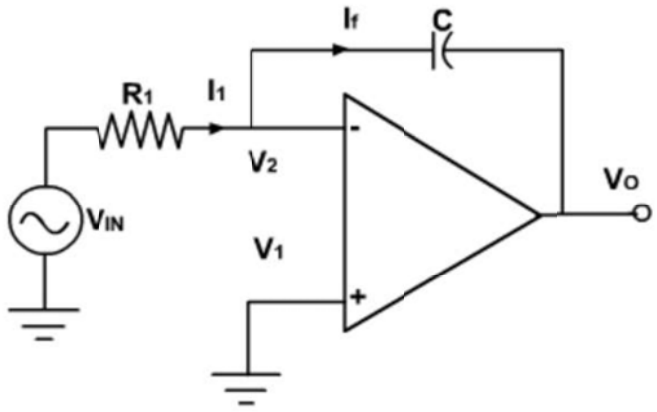


Q.5 a)

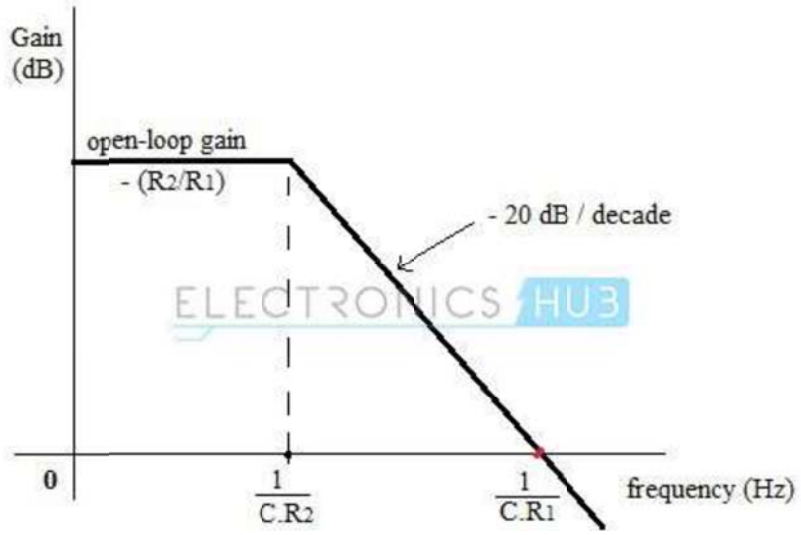


- Infinite open-loop voltage gain
- Infinite input impedance
- Zero output impedance
- Zero noise contribution
- Zero DC output offset
- Infinite bandwidth
- Differential inputs that stick together

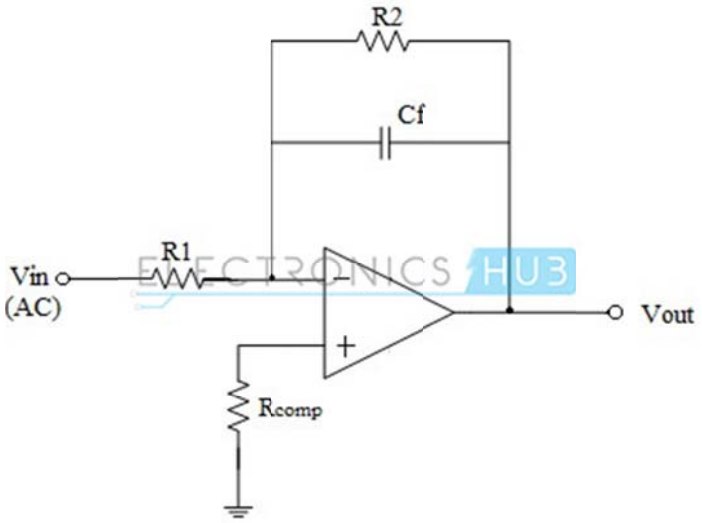
Q.5 c)



- Here, the feedback element is a capacitor. The current drawn by OPAMP is zero and also the V_2 is virtually grounded.
- Therefore, $i_1 = i_f$ and $v_2 = v_1 = 0$
- $\frac{V_{in}-0}{R} = C\frac{d(0-V_0)}{dt}$
- Integrating both sides with respect to time from 0 to t, we get
- $\int_0^t \frac{V_{in}}{R} dt = \int_0^t C\frac{d(-V_0)}{dt} dt = C(-V_0) + V_0|_{t=0}$
- If $V_0|_{t=0} = 0V$, then
- $V_0 = \frac{-1}{R}\int_0^t v_{in} dt$



Practical Integrator



Q.6 a)

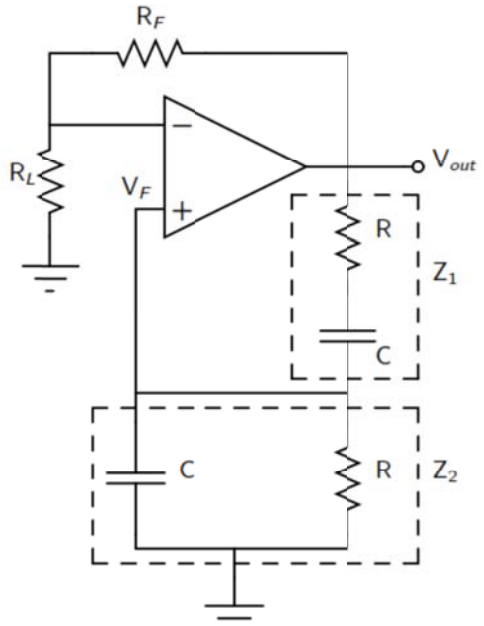
□ From the basic feedback equation $A_f = \frac{A}{1+\beta A}$

□ With Aβ=-1 and the term in the denominator becomes zero, then Af becomes infinite.

□ Therefore, an infinitesimal signal (noise voltage) can produce an output signal even without an input signal and the circuit acts as an oscillator.

 The oscillations will not be sustained if, the magnitude of the product of the transfer gain amplifier and the magnitude of feedback factor of the feedback network is less than unity.
 The condition IAβI = 1 is called the Barkhausen criterion.

Wien Bridge Oscillator



The feedback voltage V_f is given by,

$$V_f = \frac{Z_1}{Z_1+Z_2} V_{out} \qquad (1)$$

$$Z_1 = \frac{R}{1+RCS} \qquad (2)$$

$$Z_2 = R + \frac{1}{Cs} \qquad (3)$$

$$V_f = \frac{\frac{R}{1+RCs}}{\frac{R}{1+RCs} + R + \frac{1}{Cs}} V_{out}$$

Substituting the value of s=jω and simplifying we get,

$$V_f = \frac{j\omega CR}{1+3RCj\omega - C^2R^2\omega^2} V_{out} \qquad (4)$$

To ensure phase shift of 0^0 by the feedback network,

$$1 - C^2R^2\omega^2 = 0$$

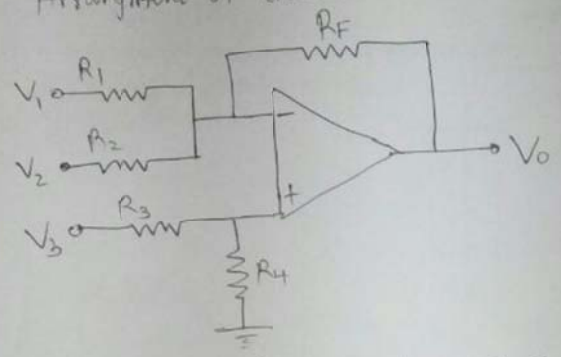
This leads to $$\omega = \frac{1}{RC} \Rightarrow f = \frac{1}{2\pi RC}$$

This happens for $$V_f = \frac{V_{out}}{3}$$

Q.6 b)

Q.6 b) Expression is $-4V_1 - 6V_2 + 4V_3 = V_o$

Arrangment of circuit is as shown.



Design R_1 & R_2 first. assuming suitable R_F

Vsing, $V_o = -\left(\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2\right)$ & $R_F = 62\,K\Omega$

$R_1 = 15\,K\Omega$ & $R_2 = 10\,K\Omega$

For designing R_3 & R_4, use superposition thm,

$\therefore V_o = \left(1 + \frac{R_F}{R_{12}}\right)\left(\frac{R_4}{R_4 + R_3}\right)V_3$ ... $\left[R_{12} = R_1 \| R_2 = 6\Omega\right]$

$\therefore 4V_3 = \left(1 + \frac{62}{6}\right)\left(\frac{R_4}{R_4 + R_3}\right)$

Assuming $R_4 = 10K$, R_3 is found to be $17.5K$

$\therefore R_3 \approx 18K$