(2½ Hours) **[Total Marks: 75]**

N. B.: (1) **All** questions are **compulsory**.
(2) Make **suitable assumptions** wherever necessary and **state the assumptions** made.
(3) Answers to the **same question** must be **written together**.
(4) Numbers to the **right** indicate **marks**.
(5) Draw **neat labeled diagrams** wherever **necessary**.
(6) Use of **Non-programmable** calculators is **allowed**.

1.	**Attempt *any three* of the following:**	**15**
a.	**Explain different constituents of microprocessor system. Draw a neat diagram showing microprocessor based system with bus architecture** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **1.1** **Memory -1M** **Input/Output – 1M** **MPU – ALU, CU, Registers – 2M** **Diagram – 2 M**	
b.	**Explain the difference between 8085 machine language and 8085 assembly language.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **1.2.2 and 1.2.3** **machine language – binary format, instruction based on bit pattern, monitor program translates keys to bit pattern – 2M** **assembly language – instructions as mnemonics, needs assembler program, instructions are human readable – 2M** **one example each – 1M** **[machine language – 0011 1100 (3C)** **assembly language - INR A (hex code 3C)]**	
c.	**With neat labled diagram explain how 8085 system bus is divided into three different sets of communication lines** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **3.1.1** **Figure 3.1 – 2 M** **Address bus, Data bus control bus – 1M each** **Expected – size of each bus and data flow bidirectional / unidirectional**	
d.	**Illustrate the memory address range of a memory chip with 256 bytes of memory. Draw a neat diagram to show the memory map and explain how this memory chip is accessed by 8085 microprocessor.**	

	Ans Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **Example 3.1** **Figure 3.10 – 2 M (any one RAM or ROM can be used. i.e. only write or both read and write control signals can be used.)** **Explanation on Use of address lines A_0 to A_7 to address memory locations 0 to 255 and together A_8 to A_{15} to select the chip – 2M** **Memory range 0000 H to 00FF H – 1 M**	
e.	**Explain how lower order data and address bus of 8085 microprocessor are demultiplexed.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **4.1.3** **Diagram showing all components (fig 4.4) – 2 M** **Description of all components – 1M** **Explanation on use of latch – 1M** **Explanation on use of control signal ALE – 1M**	
f.	**With proper timing diagram explain memory read cycle of 8085 microprocessor.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **4.3.2** **Fig 4.12 – 3M** **Explanation on demultiplexed buses – 1M** **Explanation on generation of control signals – 1M**	
2.	**Attempt *any three* of the following:**	**15**
a.	**Explain how eight DIP switches are interfaced with 8085 microprocessor using a decoder.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **5.3.1** **Diagram showing Decoder, Buffer, DIP switches along with address and data lines – 3 M** **Explanation on use of buffer – 1M** **Port address with IN instruction – 1M**	
b.	**How is testing and troubleshooting of I/O interfacing circuit is done?** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **5.5**	

	Preliminary check – hardware connection – 1M **Use of continuous loop – 2M** **Testing of various signals – 2M**	
c.	**Discuss in brief the programming model of 8085 microprocessor.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **2.1** **Fig 2.1 (b) Programming Model – 2** **Description of -** **Registers with Accumulator – 1 M** **Flags – 1 M** **PC and SP -1M**	
d.	**What is meant by hand assembly? How is hand assembling of a program done?** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **2.4 – converting from hex to binary code** **Manual or hand assembly – 1M** **Writing a program in the form of mnemonics -1 M** **Manual look up and hand assembly -2 M** **Monitor program – 1 M**	
e.	**Explain any one arithmetic and any one logical group one byte instruction from the instruction set of 8085 microprocessor.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **6.2 and 6.3** **Instruction format – 1 M each for arithmetic and logical** **Description with manual operation – 1M each for arithmetic and logical** **Example – ½ M each for arithmetic and logical**	
f.	**Write an assembly language program to add two 8 bit numbers stored at memory locations D200 H and D300 H. Store the answer at memory location D400 H. (Hex code for the program is not expected)** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **Correct program – 2 M** **Writing the memory address as per instruction format – 1, 2 or 3 byte instruction – 1M** **Writing comments – 1M** **Final output – 1M**	

3.	**Attempt *any three* of the following:**	**15**
a.	**What are different available conditional loops in the assembly language programming for 8085?** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **6.4.3** **Branch instruction – 1 M** **1M for each conditional branch syntax and description –** **Carry, Zero, Parity, Plus / Minus,**	
b.	**Explain following logical instructions –** **RAL and RLC** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **7.4** **Syntax and working of instructions RAL and RLC – 2 M each** **Example – ½ M each**	
c.	**What is time delay? Why is time delay needed in a program? What are different ways of generating a time delay in an assembly language program for 8085 microprocessor.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **8.1** **Time delay – 1 M** **Need of time delay in a program – 1M** **Generating time delay –** **Using a register – 1M** **Using register pair – 1M** **Loop within a loop – 1 M**	
d.	**Write an assembly language program for 8085 microprocessor to count continuously from FFH to 00H in a system with 0.05μs clock period. Set up a delay of 1 millisecond between two value.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **8.2** **Calculation of delay count – 2 M** **Mnemonics with proper loop statements and expected output – 3 M**	

e.	**What is stack? How is stack used both by microprocessor and user?** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **9.1** **What is stack? Stack pointer – 2 M** **Use of stack by users PUSH and POP instruction with example – 2 M** **Use of stack by microprocessor in subroutine – 1 M**	
f.	**Explain following instructions for 8085 microprocessor –** **Restart** **Conditional call and return.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **9.3.1 & 9.3.2** **Restart Instructions RST 0 to RST7 their use – 2M** **Conditional call and return – call instruction with all conditional flags – 2M** **Return instruction – 1M**	
b		
4.	**Attempt *any three* of the following:**	**15**
a.	**Write a 8085 assembly language to convert a 8-bit binary number to unpacked BCD.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **10.2.1** **Program with call instruction – 2m** **Subroutine for conversion with return instruction – 3M** **Note - program can also be written without a subroutine**	
b.	**What is meant by table look up technique? How is it used for BCD to Seven Segment LED code conversion?** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **10.3** **Look up table technique – definition and use – 2M** **Sample code – 2 M** **Output – 1 M**	
c.	**Explain the hardware features of a typical software development system.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **11.1.1**	

	HDD – 2M **SSD – 1M** **Removable Storage media – 2M**	
d.	**What are advantages of an assembler?** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **11.3.3** **Any five advantages can be listed for 1 M each.**	
e.	**Discuss various interrupts used by 8085 microprocessor and their priorities.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **12.1.3** **List of interrupts – 2M** **Priorities – 1M** **Use of priority encoder – 1M** **Interrupt Acknowledgement – 1M** **(diagram is not mandatory)**	
f.	**What is meant by vectored interrupt? Also explain use of SIM instruction.** **Ans** Microprocessors Architecture, Programming and Applications with the 8085. – Ramesh Gaonkar **12.3** **Vectored interrupts – 2M** **SIM instruction and its interpretation– 2M** **Functions of SIM -1M**	
5.	**Attempt *any three* of the following:**	**15**
a.	**What are special Pentium Registers? Discuss the architecture of Special Pentium Registers.** **Intel Book – Chapter 18** **18.2** **Diagram – 1 M** **Control register – 2M** **FLAG register – 2 M**	
b.	**Discuss the memory map of Pentium 2 processor** **Ans** **Intel Book Chapter 19** **Diagram of memory map – 3M** **Explanation – 2M**	
c.	**Explain the CPUID instruction used by Pentium 4.**	

	Ans **Intel Book Chapter 19** **Function of CPUID instruction – 2M** **Output of the instruction – 2M** **Example – 1 M**	
d.	**What is SPARC architecture based on? Explain the components of SPARC system.** **Ans** The SPARC architecture manual version 8 chapter 2 1.1 and 1.2 **SPARC architecture is based on RISC, explanation on RISC – 2M** **Components of SPARC – MMU, Supervisor software, memory model – 3M**	
e.	**List the components of SPARC processor. Discuss each in brief.** **Ans** The SPARC architecture manual version 8 chapter 2.1 **User and supervisor mode,** **Integer Unit – 1M** **Floating Point Unit – 2 M** **Co-processor – 2M**	
f.	**Explain the concept of windowed register of SPARC microprocessor.** **Ans** **The SPARC architecture manual version 8 chapter 4.1** **Windowed r register concept – 1M** **Window addressing – 2M** **Overlapping windows – 2M**	