Q. P. Code: 35366

Duration:3 hours **Total marks:80**

N.S.: (1) Question No.1 is compulsory.
(2) Solve any three from remaining five questions.
(3) Figures to the right indicate full marks

Q. 1 Answer the following questions: (20)
(a)Write the entity declaration in VHDL for NOR gate.
(b) Add $(22)_{10}$ to $(56)_{10}$ in BCD.
(c) Convert decimal 57 into binary, base 7and Hexadecimal.
(d) Construct Hamming code for 1010.
(e) Perform subtraction using 2's complement for $(10)_{10}$-$(7)_{10}$
(f) State and prove De Morgan's law.
(g) Convert $(77)_{10}$ into Excess-3 code.
(h) Perform addition of $(34)_8$ and $(62)_8$
(i)Find 8's complement of the numbers $(37)_8$ and $(301)_8$
(j)Explain ASCII code in brief.

Q. 2(a) Simplify the following equation using K map to obtain SOP equation and realize the minimum equation using only NAND gates.
$F(A,B,C,D)=\sum m(1,2,4,6,9,10,12,14) + d(3,7,13)$ (10)
(b) Implement full adder using 8:1 mux. (10)

Q. 3(a) Obtain the minimal expression using QuineMc-Cluskey method
$F(A,B,C,D)=\sum m(1,2,3,5,6,10,11,13,14) + d(4,7)$ (10)
(b) What is race around condition? How to overcome it? (10)

Q. 4(a) Design 3 bit asynchronous counter and draw the timing diagram. (10)
(b) Convert JK flipflop to SR flipflop and D flipflop. (10)

Q. 5(a) Compare TTL and CMOS with respect to different parameters. (10)
(b) Explain the features of VHDL and its modeling styles. (10)

Q. 6 Write short notes on(any four) (20)
a) Moore and Mealy machine
b) Sequence generator
c) Universal shift register
d) Priority encoder
e) Carry look ahead adder

****