QP CODE : 27812

(3 Hours) **Marks : 80**

NB : (1) **Q.1** is **Compulsory.**
(2) Attempt **any three** questions out of remaining **five**.
(3) Draw neat labelled diagram wherever necessary.
(4) For layouts use graph paper.
(5) Assumptions should be clearly mentioned.

1.
(a) Differentiate between behaviour, data flow and structural style of architecture in VHDL. **5**
(b) Write VHDL code for 2:4 decoder using process statement in behavioral style modelling. **5**
(c) What is meant by latch up in CMOS. **5**
(d) Explain various MOS capacitance. **5**

2. (a) Explain the architecture of FPGA. Explain the configurable logic block and input output block (IOB) of XC 4000 FPGA **10**
(b) What are the various types of operators used in VHDL. **5**
(c) Explain briefly various data types used in VHDL. **5**

3. (a) Write VHDL code for 4 bit full adder. **10**

(b) PMOS transistor was fabricated on n-type substrate with bulk doping density of $N_D=10^{16}/cm^3$, gate doping density (n-type poly) of $N_D = 10^{20}/cm^3$, $N_{ox} = 4 \times 10^{10}/cm^2$ and oxide thickness of $t_{ox} = 0.1\mu m$. Calculate the threshold voltage at room temperature. $\varepsilon_{si} = 11.7 \times \varepsilon_0$, $\varepsilon_{ox} = 3.97 \times \varepsilon_0$, $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm. **10**

4. (a) Design the circuit described by the function $y = \overline{(D + E + A)(B + C)}$ using CMOS and NMOS logic also draw stick diagram. **10**

(b) Compare the constant voltage and constant field scaling. Show analytically how drain current, power dissipation and power density affected by the scaling. **10**

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5. Explain briefly the following semi conductor manufacturing process. **20**
   (a) Oxidation
   (b) Diffusion
   (c) ion implantation
   (d) metalisation
   (e) etching

6. (a) Draw the circuit diagram, stick diagram and λ- based layout for 2 input NOR gate with depletion MOSFET as load, with aspect ratio of driver is 1:2 and load is 2:1. **10**

   (b) Draw the transfer characteristic of CMOS inverter and explain the operating regions of NMOS and PMOS transistor at various point in transfer characteristics. **5**

   (c) What is meant by noise margin in invertor. **5**
