Duration: 3 Hours Marks: 80

Note: (1) Question No.1 is compulsory.
(2) Attempt any three out of remaining.
(3) Assume suitable data wherever required.

Q.1	Solve any four	
(a)	Compare CMOS Technology with BJT Technology	5
(b)	Determine intrinsic gate capacitance with t_{ox} =150A^0 and W=4μm ,L=2 μm (ε_0=8.854x10^{-14}F/m & ε_{sio2}=3.9)	5
(c)	Differentiate between Static & Dynamic RAM cells.	5
(d)	Draw CMOS implementation of D Flip Flop.	5
(e)	Implement Y = using $\overline{(A+B)\bullet(C+D)}$Dynamic CMOS logic.	5
Q.2 (a)	Compare various loads used in Inverter circuit and compare different parameters which characterize each type of Inverters	10
Q.2(b))	Implement 4:1 Multiplexer using NMOS Pass Transistor Logic. Explain advantages of using Transmission gates.	10
Q3 (a)	Compare Ripple carry adder and carry look ahead adder (CLA). Explain 4 bit CLA adder implementation	10
Q3 (b)	Draw 4X4 NOR based ROM array circuitry stored following data 1011,1001,0011,0001	10
Q.4(a)	Explain clock generation networks and distribution networks used in VLSI circuits.	10
Q4 (b)	Explain Pseudo NMOS Logic and hence implement 2 I/P NAND gate.	10
Q.5(a)	Give and Explain interconnect scaling with its width ,length ,thickness and Capacitances	10
Q.5(b)	Explain various ESD protection schemes	10
Q.6	Write a short notes on (1)Sense Amplifier (2)Barrel Shifter (3) Cross talk (4) Level 1 and Level2 MOS Model	20

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