(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) **Solve** any **three** questions from remaining **five** questions.
(3) Draw neat **diagrams** and assume suitable **data** wherever **necessary**. Justify your **assumptions**.

1. (a) Explain Shift register and its applications. **5**
   (b) Explain drawback of synchronous counter. **5**
   (c) Draw truth table and circuit of Half Adder. **5**
   (d) What do you mean by noise margin ? What is its value in TTL and CMOS family ? **5**

2. (a) Simplify following function and realize using NOR gate **10**
   $$F = \Pi M(1, 2, 4, 7, 11, 13) \, d(9, 15)$$
   (b) Design Mod 5 asynchronous counter and explain glitch problem. **10**

3. (a) Design and explain 8 bit binary added using IC 7483. **10**
   (b) Analyze the sequential state machine shown in figure. Write the state table and state diagram for the same : **10**
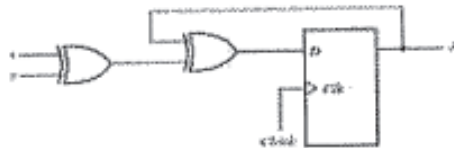
4. (a) Design a circuit with PLA to implement the following functions : **10**
   $$F1 = \Sigma m \, (1, 2, 3, 6, 9, 11)$$
   $$F2 = \Sigma m \, (2, 12, 13)$$
   $$F2 = \Sigma m \, (1, 2, 8, 12, 13)$$
   (b) Draw logic diagram of mod·8 binary counter. Sketch the resulting state variable output. **10**

5. (a) Design Moore sequence detector to detect sequence . . . . 101 . . . using D FF. **10**
   (b) Draw a circuit diagram of CMOS inverter and explain its operation. Draw its transfer characteristics. **10**

6. Write short notes on any **three** of the following :— **20**
   (a) K-map
   (b) Mealy and Moore sequential machine
   (c) Noise Margin
   (d) XC 9500 CPLD family.

_____