

(1)

SOLUTION

QP Code- 34951

Total Marks-80

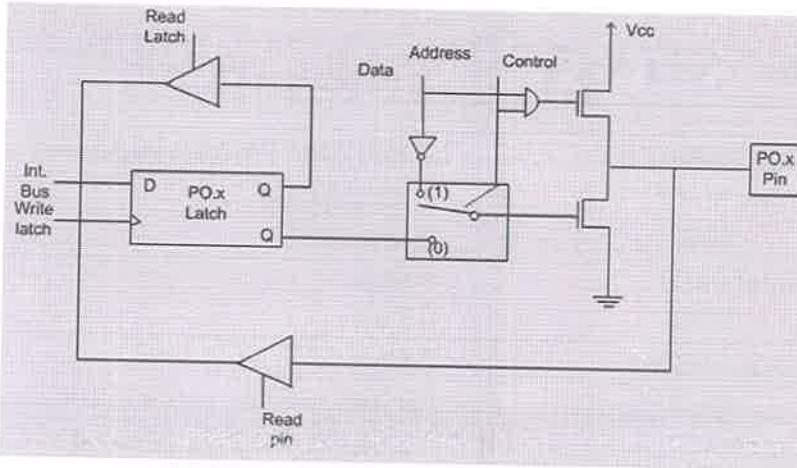
Q.1 c)	Intel 4004	4 bit (2300 PMOS transistors)	1971
	Intel 8080 8085	8 bit (NMOS) 8 bit	1974
	Intel 8088 8086	16 bit 16 bit	1978
	Intel 80186 80286	16 bit 16 bit	1982
	Intel 80386	32 bit (275000 transistors)	1985
	Intel 80486 SX DX	32 bit 32 bit (built in floating point unit)	1989
	Intel 80586 I MMX Celeron II III IV	64 bit	1993 1997 1999 2000
	Z-80 (Zilog)	8 bit	1976
	Motorola Power PC 601 602 603	32-bit	1993 1995

- d) ORG 0000H ; Set program counter 0000H
 MOV DPTR, #1000H ; Copy address 1000H to DPTR
 CLR A ; Clear A
 MOV R6, #0AH ; Load 0AH to R6
 again: MOVX @DPTR,A ; Clear RAM location pointed by DPTR
 INC DPTR ; Increment DPTR
 DJNZ R6, again ; Loop until counter R6=0
 END

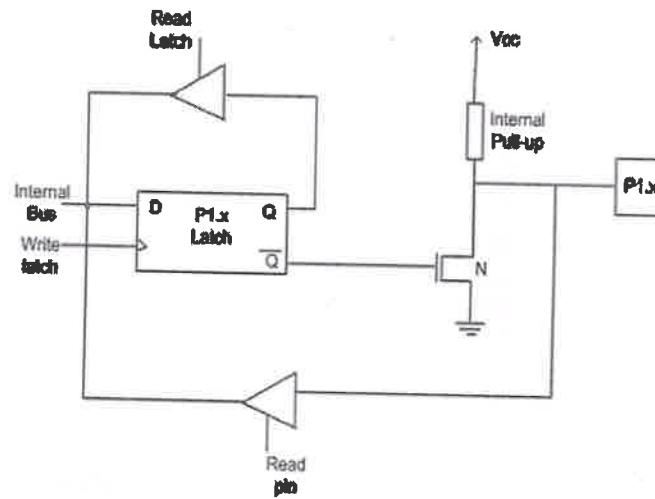
- Q.2 a) ORG 0000H ; Set program counter 00 OH
 MOV A, 70H ; Load the contents of memory location 70h into A
 MOV B, 71H ; Load the contents of memory location 71H into B
 MUL AB ; Perform multiplication
 MOV 52H,A ; Save the least significant byte of the result in location 52H
 MOV 53H,B ; Save the most significant byte of the result in location 53
 END

O2

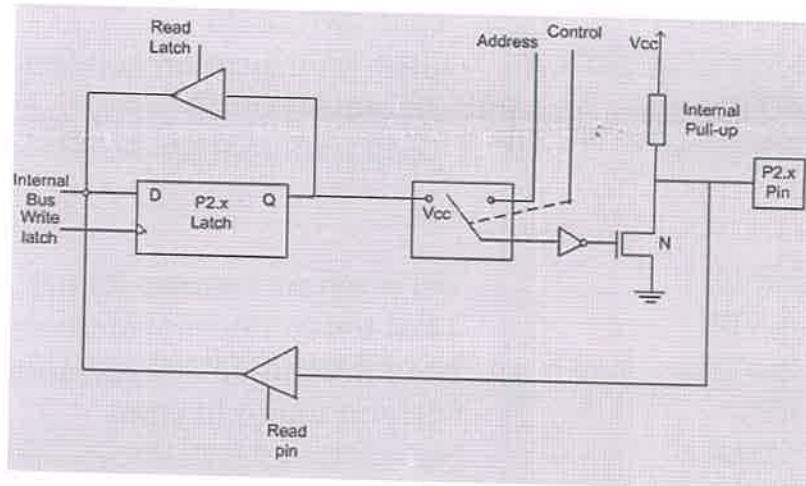
b) Port 0 structure-



Port 1 structure-

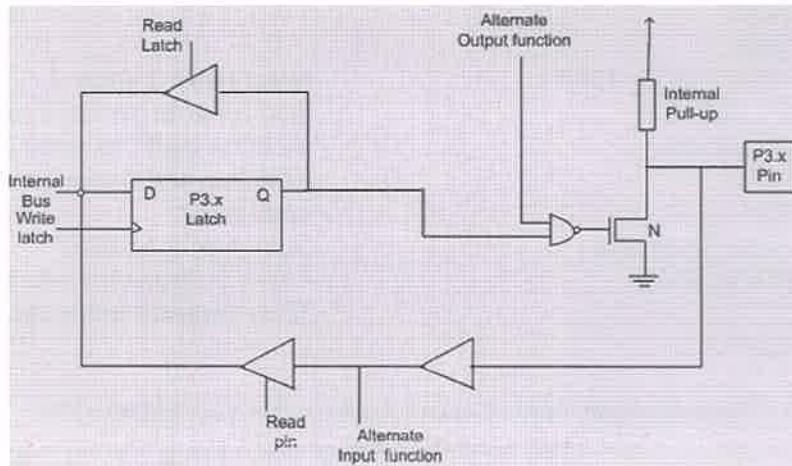


Port 2 structure-



(Q3)

Port 3 structure-



Alternate functions of Port-3 pins are -

P3.0	RxD
P3.1	TxD
P3.2	INT0
P3.3	INT1
P3.4	T0
P3.5	T1
P3.6	WR
P3.7	RD

- Q.3 b) The period of the square wave is
 $T = 1/(2 \text{ kHz}) = 500 \mu\text{s}$.
 Each half pulse = $250 \mu\text{s}$.
 The value n for $250 \mu\text{s}$ is: $250 \mu\text{s} / 1 \mu\text{s} = 250$
 $65536 - 250 = \text{FF06H}$.
 $\text{TL} = 06\text{H}$ and $\text{TH} = 0\text{FFH}$.

MOV TMOD,#10 ;	Timer 1, mode 1
AGAIN: MOV TL1,#06H ;	TL0 = 06H
MOV TH1,#0FFH ;	TH0 = FFH
SETB TR1 ;	Start timer 1
BACK: JNB TF1,BACK ;	Stay until timer rolls over
CLR TR1 ;	Stop timer 1
CPL P1.5 ;	Complement P1.5 to get Hi, Lo
CLR TF1 ;	Clear timer flag 1
SJMP AGAIN ;	Reload timer



Q.4 a)

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ORG 0000H
LJMP START
ORG 0030H
START: MOV TMOD, #20H ; select timer 1 mode 2
        MOV TH1, #0FAH ; load count to get baud rate of 4800
        MOV SCON, #50H ; initialize UART in mode 2
        ;
        SETB TR1 ; 8 bit data and 1 stop bit
AGAIN: MOV SBUF, #'A' ; start timer
        BACK: JNB TI, BACK ; load char 'A' in SBUF
        CLR TI ; Check for transmit interrupt flag
        SJMP AGAIN ; Clear transmit interrupt flag
END

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b)

TMOD : Timer/Counter Mode Control Register (Not Bit Addressable)

GATE	C/T	M1	M0	GATE	C/T	M1	M0

TIMER 1

TIMER 0

GATE When TRx (in TCON) is set and GATE = 1, TIMER/COUNTERx will run only while INTx pin is high (hardware control). When GATE = 0, TIMER/COUNTERx will run only while TRx = 1 (software control).

C/T Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).

M1 Mode selector bit (NOTE 1).

M0 Mode selector bit (NOTE 1).

Note 1 :

M1	M0	OPERATING MODE
0	0	13-bit Timer
0	1	16-bit Timer/Counter
1	0	8-bit Auto-Reload Timer/Counter
1	1	Timer 0: TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit Timer and is controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter 1 stopped.

TCON Register

TCON : Timer/Counter Control Register (Bit Addressable)

TT1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1 TCON.7 Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine.

TR1 TCON.6 Timer 1 run control bit. Set/cleared by software to turn Timer/Counter ON/OFF.

TF0 TCON.5 Timer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as processor vectors to the service routine.

TR0 TCON.4 Timer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF.

IE1 TCON.3 External Interrupt 1 edge flag. Set by hardware when External interrupt edge is detected. Cleared by hardware when interrupt is processed.

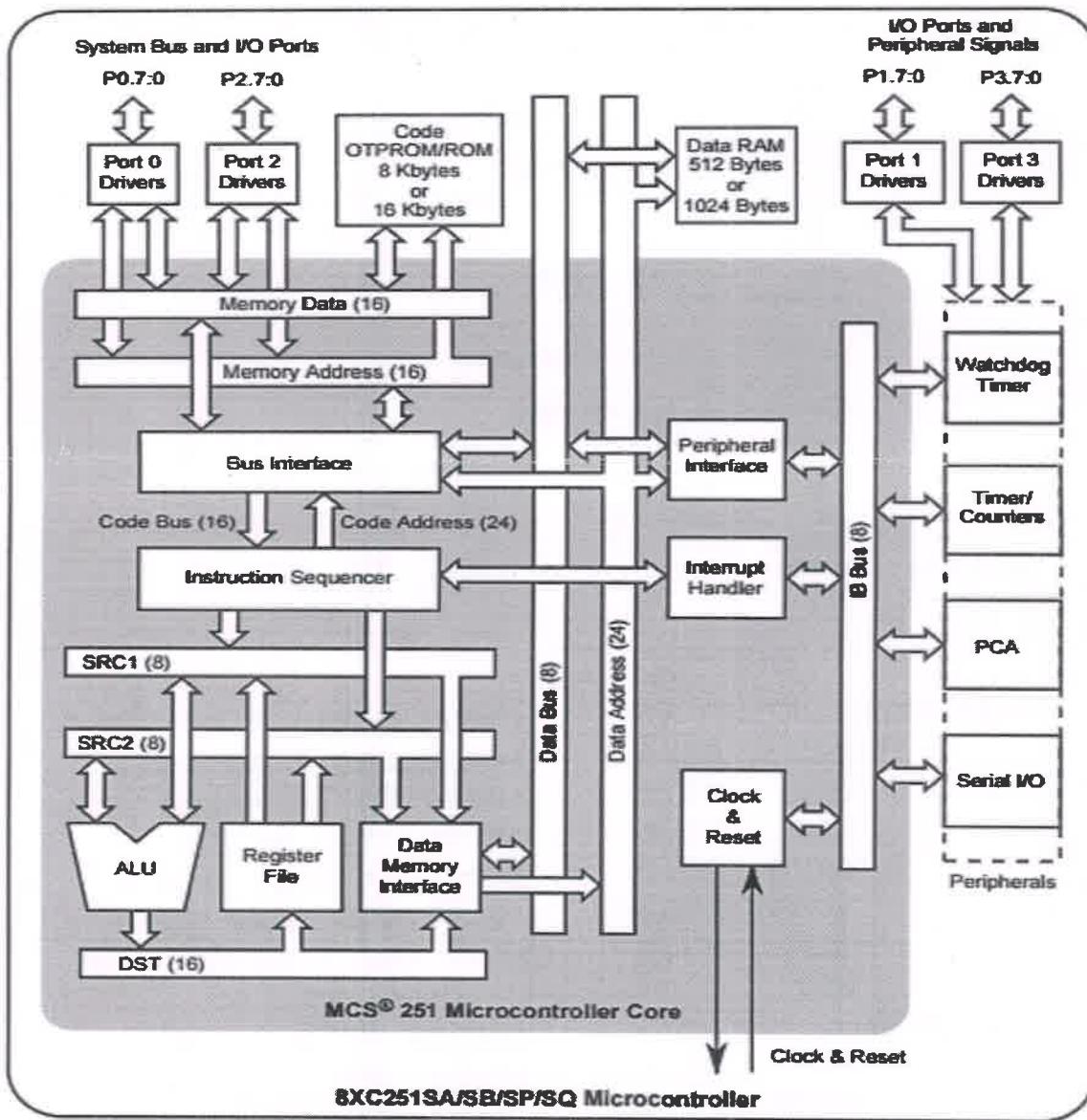
IT1 TCON.2 Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.

IE0 TCON.1 External Interrupt 0 edge flag. Set by hardware when External interrupt edge detected. Cleared by hardware when interrupt is processed.

IT0 TCON.0 Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.

Q5

Q.5 a)



Q6

b) ;Call a time delay before sending next data/command
; P1.0-P1.7=D0-D7, P2.0=RS, P2.1=R/W, P2.2=E

```
        ORG      0
        MOV      DPTR, #MYCOM
C1:      CLR      A
        MOVC    A, @A+DPTR
        ACALL   COMNWRT ;call command subroutine
        ACALL   DELAY   ;give LCD some time
        INC     DPTR
        JZ      SEND_DAT
        SJMP   C1

SEND_DAT:
        MOV      DPTR, #MYDATA
D1:      CLR      A
        MOVC    A, @A+DPTR
        ACALL   DATAWRT ;call command subroutine
        ACALL   DELAY   ;give LCD some time
        INC     DPTR
        JZ      AGAIN
        SJMP   D1
AGAIN:   SJMP   AGAIN    ;stay here
* * * * *

* * * *
COMNWRT:           ;send command to LCD
        MOV      P1,A      ;copy reg A to P1
        CLR      P2.0      ;RS=0 for command
        CLR      P2.1      ;R/W=0 for write
        SETB    P2.2      ;E=1 for high pulse
        ACALL   DELAY   ;give LCD some time
        CLR      P2.2      ;E=0 for H-to-L pulse
        RET

DATAWRT:           ;write data to LCD
        MOV      P1,A      ;copy reg A to port 1
        SETB    P2.0      ;RS=1 for data
        CLR      P2.1      ;R/W=0 for write
        SETB    P2.2      ;E=1 for high pulse
        ACALL   DELAY   ;give LCD some time
        CLR      P2.2      ;E=0 for H-to-L pulse
        RET

DELAY:   MOV      R3,#250 ;50 or higher for fast CPUs
HERE2:   MOV      R4,#255 ;R4 = 255
HERE:    DJNZ   R4,HERE ;stay until R4 becomes 0
        DJNZ   R3,HERE2
        RET

ORG      300H
MYCOM:  DB      38H,0EH,01,06,84H,0 ; commands and null
MYDATA: DB      "HELLO",0
        END
```

07

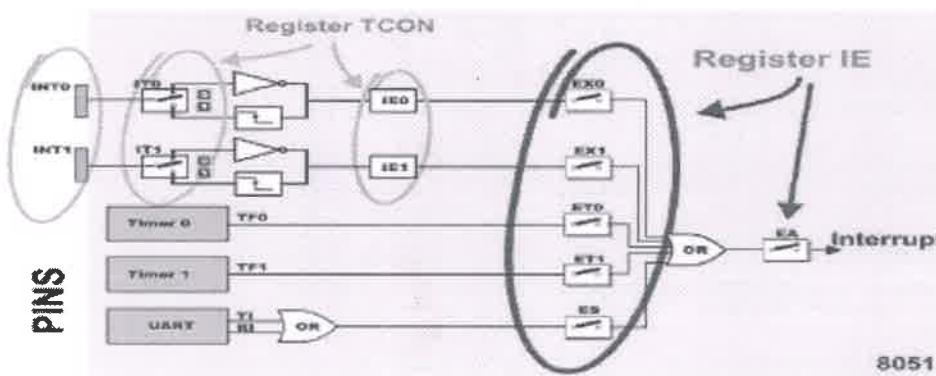
Q.6 a)

```

ORG 0000H
MOV R1,#N
MOV A,R1
MOV B,R1
MUL AB           //SQUARE IS COMPUTED
MOV R2, B
MOV B, R1
MUL AB
MOV 50,A
MOV 51,B
MOV A,R2
MOV B, R1
MUL AB
ADD A, 51H
MOV 51H, A
MOV 52H, B
MOV A, # 00H
ADDC A, 52H
MOV 52H, A       //CUBE IS STORED IN 52H,51H,50H
END

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b)



	0	X	0	0	0	0	0	Value after Reset
IE	EA	b16	ET2	ES	ET1	EX1	ET0	EX0
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

	X	X	0	0	0	0	0	Value after Reset
IP			PT2	PS	PT1	PX1	PT0	PX0
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

