N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions from the remaining five.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt any 5 questions [20]

a) Prove that for a JFET the gate-source bias for zero temperature drift of drain current is at $|V_{GR}| = 0.63$ volts.

b) Explain the hybrid pi model of BJT.

c) Explain Zener as voltage regulator.

d) Consider a BJT has parameters $f_T = 500$MHz at $I_C = 1mA$, $\beta = 100$ and $C_{eu} = 0.3pF$. Calculate bandwidth of $f_B$ and capacitance $C_T$ of a BJT.

$\text{DATA:}$
$\begin{align*}
\text{f}_T &= 500\text{MHz} \\
I_C &= 1\text{mA} \\
\beta &= 100 \\
C_{eu} &= 0.3\text{pF}
\end{align*}$

$\text{To FIND:}$
$\begin{align*}
f_B \\
C_T
\end{align*}$

$\text{SOLUTION:}$

$\text{STEP 1:}$
$\frac{f_B}{f_T} = \frac{500 \times 10^6}{100} = 5\text{MHz}$

$\text{f}_B = 5\text{MHz}$

$\text{STEP 2:}$
$\gamma_m = \frac{I_C}{\beta} - \frac{1 \times 10^{-3}}{26 \times 10^{-9}} = 38.5 \text{mV}$

$\text{STEP 3:}$
$\frac{f_T}{\gamma_m} = \frac{500 \times 10^6}{38.5 \times 10^{-3}} = \frac{10\times 10^{12}}{C_T + C_{eu}}$

$C_T = 0.12\text{pF}$

e) Draw and explain small signal model of a diode.

\[ 
\begin{array}{c}
\text{Diode} \\
\text{v}_D(t) \\
+ \\
V_D \\
- \\
\text{v}_D(t)
\end{array} \]
Q.2  a) Design a voltage divider bias network using a supply of 24 V, a transistor \[ \beta = 110 \] and an operating point of \( I_C = 4 \) mA and \( V_{CEO} = 8 \) V.

Assume \( V_E = \frac{1}{8} V_C \).

**STEP 1:** KVL to open loop.

\[ V_{CC} - I_C R_C - V_{CE} - V_E = 0 \]

\[ R_C = 3.25 \text{ k} \Omega \]

**STEP 2:**

\[ V_E = I_B R_E \]

\[ R_E = 470 \text{ k} \Omega \]

**STEP 3:**

\[ V_{TH} = I_B R_{TH} - V_{BE} - V_E = 0 \]

\[ V_{TH} = \frac{R_2}{R_1 + R_2} \times 24 \]

\[ R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \]

\[ V_{TH} = \frac{R_{TH} \times 24}{R_1} \Rightarrow R_{TH} = \frac{V_{TH} R_1}{24} \]

Let \( R_1 = 10k \)

\[ V_{TH} = 3.756 \text{ V} \]

\[ R_{TH} = \frac{3.756 \times 10k}{24} \]

\[ R_{TH} = 1.565 k \]

\[ R_{TH} = \frac{10k \times R_2}{10k + R_2} \]

\[ R_2 = 1.855k \]

b) Explain the fabrication steps of passive elements.

Fabrication Steps are:
Silicon Wafer preparation, Epitaxial Growth, Oxidation, Diffusion, Ion implantation, Isolation technique, Metallization, Assembly processing and packaging.
c) What are the important JFET parameters and define it from characteristics.  

Drain resistance \( r_d = \frac{\Delta V_{DS}}{\Delta I_D} \)

Transconductance \( g_m = \frac{\Delta I_D}{\Delta V_{GS}} \)

Amplification factor \( \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = (\Delta V_{DS} / \Delta I_D) \times (\Delta I_D / \Delta V_{GS}) = r_d \times g_m \)

Q.3

a) Design the resistors of a single stage CS amplifier for audio frequency with BFW11 with \( I_{DS} = (3.3 \pm 0.6) \text{mA} \) and \( |A_V| = 12 \).

**STEP 1: DATA FROM DATASHEET**

- \( I_{DS} = 3 \text{mA} \)
- \( g_m = 5000 \mu \text{S} \)
- \( V_P = -2.5 \text{V} \)
- \( r_d = 50 \text{k}\Omega \)

**STEP 2: SELECTION OF BIASENG TECHNIQUE**

Since variation in parameter is given, we will select potentiometer biasing.

**STEP 3: CALCULATION FROM GRAPH OF TRANSFER CHARACTERISTICS**

We observe that the graph to be taken from the datasheet mentioned as JFET mutual characteristics.

From graph \( V_G = 2.9 \text{V} \) and \( \frac{V_G}{R_S} = 2.4 \text{mA} \)

\[ V_G = \frac{V_G}{R_S} = \frac{2.9}{2.4} \text{mA} = 1.29 \text{k}\Omega \]

Let \( R_S = 1.2 \text{k}\Omega \)

\[ V_{GB} = V_G - I_D \times R_S \]

\[ I_{DS} = \frac{I_{D(max)} - I_{D(min)}}{2} = \frac{3.9 \text{mA} + 2.4 \text{mA}}{2} = 3.3 \text{mA} \]
8. STEP 5: CALCULATION OF $R_D$
   $I_{AV} = g_m \frac{V_D}{R_D}$

STEP 6: CALCULATION OF $V_{DSQ}$
   Since $V_D$ is not given, let $V_D = \sqrt{2}$.
   $V_{DSQ} = 1.5 \left( V_{D(p)} + IV_{P1} \right)$

STEP 7: CALCULATION OF $V_{DD}$
   $V_{DD} = I_{DQ} (R_3 + R_D) + V_{DSQ}$

STEP 8: CALCULATION OF $R_1$ and $R_2$
   $V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2}$
   $\frac{R_1}{R_2} = \frac{V_{DD}}{V_G}$

b) Draw CS JFET amplifier with self bias circuit and derive the expression for voltage gain input impedance and output impedance.

i) Circuit Diagram
ii) Small Signal Hybrid Pi model
iii) Derivation of expression of voltage gain, input resistance and output resistance

Q.4 a) Draw small signal hybrid parameter equivalent circuit for CE amplifier and define the same. What are the advantages of h parameters?

Mention advantages of h parameters

b) For the circuit shown below in Fig.4b, the transistor parameters are $V_{BE(0)} = 0.7$ V, $\beta = 200$ and $V_A = \infty$.

i) Derive the expression for lower cut-off frequency (or time constant) due to input coupling capacitor.
ii) Determine lower cut-off frequency and midband voltage gain.
DC Analysis (calculate $g_m$ and $r_s$)

AC analysis

Derivation of expression for time constant

$$\tau_s = (R_s + \omega C)$$. \( C \)

$$\frac{1}{\omega L} = \tau_s$$

$$\left| A_V(m) \right| = \frac{g_m R_c R_e}{(R_s + \omega i) (R_e + \omega L)}$$

Q.5 a) Design an L section LC filter with full wave rectifier to meet the following specifications: The DC output voltage \( V_{DC} = 220 \text{ V} \), deliver \( I_L = (70 \pm 20) \text{ mA} \) to the resistive load and the required ripple factor is 0.04.

$$\text{Ripple factor} \quad \gamma = \frac{1}{G \sqrt{2} \omega L C}$$

Critical inductance \( L_c = \frac{R_L}{3\omega} \)

$$R_L = \frac{V_{DC}}{I_L}$$

Calculate value of $L$ and using formula of ripple factor calculate value of $C$.

b) For the circuit shown below in Fig.5b, the transistor parameters are \( V_{BE(on)} = 0.7 \text{ V}, \beta = 100 \) and \( V_A = \infty \). Determine $Z_i$, $Z_o$ and $A_V$.
STEP 1: DC ANALYSIS

STEP 2: AC ANALYSIS

Hybrid pi equivalent circuit

\[ V_o = -g_{mV} \left( \frac{2.7k || 1k}{1+\beta} \right) \]

\[ R_i = \frac{\tau_{\pi}}{1+\beta} \]

\[ R_o = 2.7k || 1k \]

Q.6 Short notes on: (Attempt any four)
a) BJT high frequency equivalent circuit

Components of:
- a) base-emitter
- b) collector-emitter
- c) base-collector
b) Types of resistors and capacitors
   - Resistors are broadly classified into 2 categories:
     a) Fixed resistors
        Symbol: \[ \text{---} \rightarrow \text{---} \]
        They are classified as carbon composition, metalized type, wire wound type.
     b) Variable or adjustable resistors
        For circuits requiring a resistance that can be adjusted while it remains connected in the circuit (such as volume control on a radio), variable resistors are required.
        They have 3 leads, 2 fixed and one movable.

c) Stability factors of various biasing techniques of BJT
   Biasing refers to the application of D.C. voltages to setup the operating point in such a way that output signal is undistorted throughout the whole operation. Once selected properly, the Q point should not shift because of change of IC due to \( \beta \) variation due to replacement of the transistor of same type and Temperature variation.
   The process of making operating point independent of temperature changes or variation in transistor parameters is known as stabilization.
   Expression of stability factors of various biasing techniques.

d) Different types of filters
   Mention details of L, C, LC, CLC filter.

e) Comparison of BJT CE and JFET CS amplifier
   Mention 5 points of comparison.

\[
\begin{align*}
0.007 & \quad J_D = 0.0022 \ \text{gm} \\
\frac{J_D}{\text{gm}} & = 0.814 \\
J_D & = J_DSS \left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{gm} = -\frac{2J_DSS}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right) \\
\left(\frac{1 - V_{GS}}{V_P}\right) \times V_P & = 0.814 \\
-2 & \quad |V_{GS}| = |V_P| - 0.63 \\
\text{Thus} & \quad |V_{GD}| = |V_P| - 0.63
\end{align*}
\]