81.a) data in's = A, B, C
     0/1's = y_1 (msb) & y_2 (lsb)

\[
\begin{array}{c|c|c|c|c}
A & B & C & y_1 & y_2 \\
\hline
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 1 & 0 & 1 \\
0 & 1 & 0 & 1 & 0 \\
0 & 1 & 1 & 0 & 1 \\
1 & 0 & 0 & 0 & 1 \\
1 & 0 & 1 & 1 & 0 \\
1 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 1 & 1 \\
\end{array}
\]

\[y_1 = AB + AC + BC\]
\[y_2 = ABC \overline{C}\]

81.b) DeMorgan's theorems
     i) \[\overline{AB} = \overline{A} + \overline{B}\]
     proof 2 mks
     ii) \[A + \overline{B} = \overline{A} \overline{B}\]
     proof 2 mks

81.c) Steps of Quine McCluskey 4 mks
     - listing of minterms
     - group according to no. of 1's
     - form 1st & 2nd reduction tables
     - cover table & choose columns & get the answer

81.d) 4:1mux 4 mks
     - diagram
     - truth table & equations
     - explanation
     - circuit diagram

81.e) Weighted codes 4 mks
     - explanation
     - examples
     - eg. binary code (8,4,2,1 weights)
8.1.4. Parity
- Explanation
- Even & odd parity
- Error detection by parity
- Eg. Hamming code

8.2 a) SR Flip Flop using NAND gates:
- Diagram
- Working of the F/F
- Truth table
- Characteristic equation

8.2 b) 4 bit Gray (G3G2G1G0) code to binary (B3B2B1B0)
- Code converter:
  - Truth table 3 mks
  - K-map & equations 5 mks
  - Circuit diagram 2 mks

B3 = G3, B2 = G3 & G2, B1 = G3 & G2 & G1, B0 = G3 & G2 & G1 & G0

8.3 a) Quine McClusky's method
\[ y = f(A, B, C, D) = \sum (0, 1, 3, 4, 5, 6, 11, 13, 14, 15) \]
- Expand M (2, 7, 8, 9, 10, 12)
- List all minterms 1 mks
- Group according to no of 1's 3 mks
- Form 1st & 2nd reduction tables 2 mks
- Cover table 2 mks
- Choose columns & get the answer 2 mks

\[ y = \overline{AD} + \overline{BCD} + BCD + ABD \]
83 b) Full subtractor
- Truth table 2 mks
- K maps and equations for 3 mks
- Difference and
- Borrow
- Circuit diagram 2 mks

83 c) Universal gates 3 mks
- NAND and NOR
- Explanation about their use
  e.g. mass production, low cost of manufacturing

84 a) Binary asynchronous decade counter
- Diagram 3 mks
- Explanation 4 mks
- Timing diagram 2 mks
- Reset logic 2 mks

84 b) \( y = f(A, B, C, D) \)
\[ y = TM(1, 2, 3, 5, 6, 7, 8, 12, 13) \]
\[ y = Zm(0, 4, 9, 10, 11, 14, 15) \]

\[ D_0 = \overline{A}B + \overline{A}B = \overline{A} \]
\[ D_1 = AB \]
\[ D_2 = AB + AB = A \]
\[ D_3 = \overline{AB} + AB = A \]
85a) Logic families
   - Comparison (3) mks
   - Explanation (7) mks

85b) Serial I/O
   - Serial I/O register
     - Diagram (4) mks
     - Explanation (6) mks

86a) Counter ICs:
   - Diagram (2) mks
   - Explanation (2) mks
   - Examples (1) mks
86 (b) Hamming Code:
- explanation 3 mks
- example 2 mks

86 (c) Excess-3 Code:
- explanation 3 mks
- self-complementing code 2 mks

86 (d) Parity Generator Circuit
- at the transmitting end 2 mks
- example 1/2 mk

Parity Checker Circuit
- at the receiving end 2 mks
- example 1/2 mk

86 (e) 5 & 6 variable K-maps
- explanation 2 mks
- examples of both types of K-maps 3 mks