01 Q.P. code:- 21325

Paperset 2 Solution

Q1.a) data i/p's = A, B, C (4 mks)
o/p's = y_1 (MSB) & y_2 (LSB)

A	B	C	y_1	y_2
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$y_1 = AB + BC + AC$

$y_2 = A \oplus B \oplus C$

Q1b) DeMorgan's theorems
i) $\overline{AB} = \overline{A} + \overline{B}$ proof (2) mks
ii) $\overline{A+B} = \overline{A} \cdot \overline{B}$ proof (2) mks

Q1c) Steps of Quine McCluskey (4) mks
- listing of minterms
- group according to no. of 1's
- Form 1st & 2nd reduction tables.
- covertable
- choose columns & get the answer

Q1d) 4:1 MUX (4) mks
- diagram
- truth table & equations
- explanation
- circuit diagram

Q1.e) Weighted codes (4) mks
- explanation
- examples
  eg. binary code (8,4,2,1 weights)

Q1 f) Parity (4) mks
- explanation
- even & odd parity
- error detection by parity
- eg. Hamming code

Q2 a) SR FlipFlop using NAND gates :- (10) mks
- diagram
- Working of the F/F
- truth table
- characteristic equation
- state transition diagram
- excitation table

Q2 b) 4 bit Gray ($G_3G_2G_1G_0$) code to binary ($B_3B_2B_1B_0$) code converter :-
- Truth table (3) mks
- K maps & equations (5) mks
- circuit diagram (2) mks

$B_3 = G_3$, $B_2 = G_3 \oplus G_2$, $B_1 = G_3 \oplus G_2 \oplus G_1$, $B_0 = G_3 \oplus G_2 \oplus G_1 \oplus G_0$

Q3 a) Quine McCluskey's method

$Y = f(A,B,C,D) = \sum m\,(0,1,3,4,5,6,11,13,14,15)$

$= \Pi M\,(2,7,8,9,10,12)$

- list all minterms (1) mk
- group according to no. of 1's. (3) mks
- Form 1st & 2nd reduction tables (2) mks
- cover table (2) mks
- choose columns & get the answer (2) mks

$Y = \overline{A}\,\overline{C} + \overline{B}CD + BC\overline{D} + ABD$

03

Q3b) full subtractor (3)
- truth table (2) mks
- K maps & equations for (3) mks
  - Difference and
  - Borrow
- circuit diagram (2) mks

Q3c) Universal gates (3) mks
- NAND and NOR
- explanation about their use
  eg mass production, low cost of manufacturing

Q4a) Binary asynchronous decade counter
- diagram (2) mks
- explanation (4) mks
- timing diagram (2) mks
- Reset logic (2) mks

Q4b) $y = f(A,B,C,D)$
$= \Pi M(1,2,3,5,6,7,8,12,13)$
$= \Sigma m(0,4,9,10,11,14,15)$ (5) mks

i)

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	$\bar{A}$	A	A	A	$\bar{A}$	0	A	A

(5) mks

ii)

	D_0	D_1	D_2	D_3
$\bar{A}\bar{B}$	0	1	2	3
$\bar{A}B$	4	5	6	7
$A\bar{B}$	8	9	10	11
AB	12	13	14	15

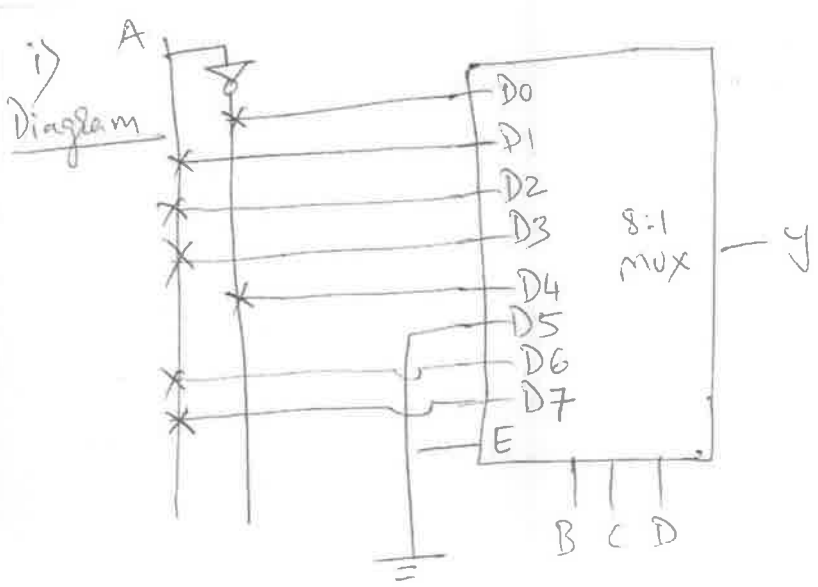
$D_0 = \bar{A}\bar{B} + \bar{A}B = \bar{A}$
$D_1 = A\bar{B}$
$D_2 = A\bar{B} + AB = A$
$D_3 = A\bar{B} + AB = A$

(5) mks

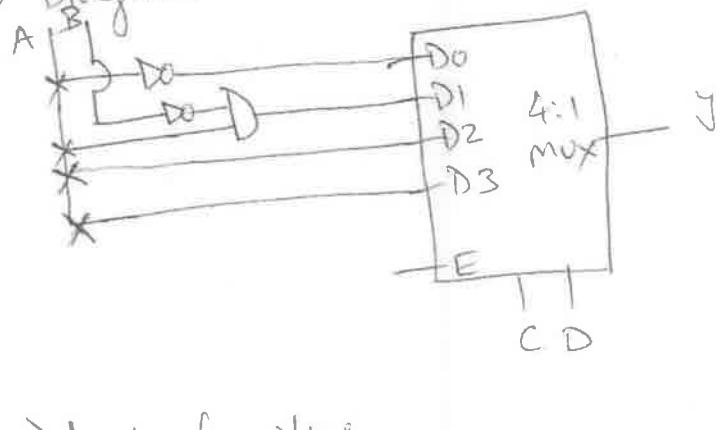
Q4

4

i) Diagram



ii) Diagram



Q5 a) Logic families
- comparison (3) mks
- explanation (7) mks

Q5 b) Serial i/p Serial o/p register
- diagram (4) mks
- explanation (6) mks

Q6. a) Counter ICs :-
- diagram (2) mks
- explanation (2) mks
- examples (1) mk

05

Q6 b) Hamming Code : (5)
- explanation (3) mks
- example (2) mks

Q6 c) Excess-3 code :
- explanation (3) mks
- self complementing code (2) mks.

Q6 d) Parity Generator Circuit
- at the transmitting end (2) mks
- example (1/2) mk

Parity Checker Circuit
- at the receiving end (2) mks
- example (1/2) mk

Q6 e) 5 & 6 variable K maps
- explanation (2) mks
- examples of both type of K-maps (3) mks